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Investigation of the Thermal Loading and Random Vibration Influences on Fatigue Life of the Solder Joints for a Metal-Oxide-Semiconductor-Field-Effect Transistor in a DC-DC Power Boost Converter

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ABSTRACT This study presents the effects of the vibration and thermal cycling on the fatigue life of a power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in a power converter circuit. The fatigue mechanism in per loading mode was investigated separately and based on the overlap approach, the synchronous effects were analyzed. The solder creeps' attitudes are depended on the fatigue life for the thermal loops. The success of the deposited strain per thermal loop is in direct relation with the fatigue lifetime. The main source of the stress in the packaging process is the differences between the components' thermal coefficients. To evaluate the effects of the vibration on the fatigue life for the solder layers, the RMS value of the peeling stress was considered. According to the results, the maximum stress and main affected points realized at the corners of the layers. It has been identified that the assembling of the thermal effects and mechanical loads are quickened the failure rate at the solder joints for this device. The Finite Element Method (FEM) is used for the simulation and the results confirm the estimated crack formation places in the layers.

INDEX TERMS Solder joints, power MOSFET, fatigue life, finite element method (FEM).

I. INTRODUCTION

Power electronics applications and designs widely are expanding based on their inevitable role in Renewable Energy Sources (RESs), industries and aerospace implementations to transmit the power to the load side [1], [2]. In recent years, many comprehensive studies are presented for DC-DC power boost converters that are the main structure between the RESs and load sides. These converters are including the power components like diode and switches. For high frequency and efficient circuits normally power MOSFETs are selected [3]–[6].

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So, the reliability and durability of the components for a power electronic circuit are the most important parameters that can increase the lifetime and decrease the fatigue of the circuit. For the fatigue analysis subject, the influence of the vibration and thermal cycling especially for the moving circuits are the focus auspices for the researchers as the main effective parameters. Under the vibrations, thermal changes and the loading, the solder joints as the main affected points in a power circuit are investigated. Based on the research results, while the crack and thermal fatigue are formed at the edges and corner sides of the solder layers, the Non-static energy is collected at the solder balls. Finite Element Method (FEM) is the most common approach for the fatigue analysis

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of the solders in an electronic package. Based on this analysis device, the reliability of an Sb-solder including the In and Bi elements is higher and improved. Individual multi-dimension models for the estimation of the cracks in a power module were investigated and examined in [7]. This technique can model the crack stream at the seed boundaries of the solders of a power module. Also, the reliability of solders under thermal loops for a microelectronic package was analyzed in [8]–[14]. This research results Show that the longest fatigue life belongs to solders including the SnAgCu (SAC) elements. The vibration effects of the solder joints are investigated as well as thermal cycling analysis [15]–[19]. A local analysis model was used in [16] to assess the random vibration effects for the dummy solder joints. According to the results of this research, the corners of an electronic package are the most affected points under vibration and locating the higher number of solder joints at the corners can decrease the useful long life and decrease the fatigue of the package. Frequency-Domain (FD) and Monte-Carlo (MC) models are the most common techniques for fatigue estimation for the solder joints under the vibration and according to the [11], [20], [21], the FD approach is more accurate. For the Plastic Quad Flat (PQF)-based Printed Circuit Boards (PCBs), based on the Boltzmann–Arrhenius–Zhukov (BAZ) model [22], [23], the cracks in the solder joints is started from the solder to the copper lead under the vibration.

Based on presented researches, the fatigue life of the solder joints is analyzed separately under vibration and thermal cycling and there is a limited number of studies that present the fatigue of the solder joints under both thermal and vibration effects. The importance of this subject when it will be more clear that understand the for many moving approaches like aerospace attempts, both of these effects are applied to the electronic device or module.

In different studies, the thermal cycling and random vibration have been analyzed separately as two different parameters for the power modules and the fatigue investigation of the solder joints in the modules under the simultaneous influences of these parameters need to be presented because normally these parameters are applied at the same time especially for the moving systems. Also, the DC-DC converters are the main structures in Renewable Energy Applications (REAs) like Photovoltaic (PV) systems and the power switches acts as the most important components in these converters are derived with different level of switching frequencies under different level of the voltages and currents. This study presents the effects of the vibration and thermal cycling on a SnAgCu (SAC) type of the solder joints for a power switch in a DC-DC Power Boost Converter separately and then, the combined effects of these parameters is analyzed.

II. FINITE ELEMENT METHOD (FEM) ANALYSIS

This section presents three different steps for vibration, thermal and combination of random vibration and the thermal cycling influences on the solder joints of a DC-DC power boost converter separately. This converter is used widely for power transmission purposes between the power sources and loads like electrical motors or electrical devices that work with DC voltages [24]–[27]. The converter includes the inductor, power switch, input, and output capacitors and connectors for the input and output source and load. For the first step, the random vibration (RV) effects are analyzed:

A. RV SIMULATION AND RESULTS

A thin rectangular isotropic plate is illustrated in Figure 1. This plate is presented to simulate an electronic board in three dimensions simply in order to obtain the amount of stress in solder joints under random vibration. As can be seen in this figure, the displacement of an any arbitrary point of the plate under the vibration can be modeled and presented by equations. This can be the first step to present the fatigue life of a solder joint on the electronics boards. Reference [29] presents a comprehensive model for the reaction of this plate. The vibration equation for that is written as (1) [28].

$$\rho\frac{\partial^2 w}{\partial t^2}+c\frac{\partial w}{\partial t}+D\nabla^4 w=0 \tag{1}$$

ρ and c respectively, are the density and the damping coefficient of the sheet relative to the surface unit. D is the flexural stiffness of the sheet. Sheet displacement is given by relation (2) [29].

$$w_a\left(x,y,t\right)=w_b\left(t\right)+w\left(x,y,t\right) \tag{2}$$

w_a and $_{\mathrm{wb}}$ are the absolute and basic or boundary displacements and w is the displacements relative to the boundary that is well known as the deflection that means the displacement of an arbitrary point on the plate. The length and width of the pale are shown by a and b. Relation (3) results from the substitution of relation (2) in relation (1) [30].

$$\rho\frac{\partial^2 w}{\partial t^2}+c\frac{\partial w}{\partial t}+D\nabla^4 w=p\left(t\right) \tag{3}$$

Assuming that relationship (3) has an answer as relationship (4), by substitution (4) into (3) one can obtain (5) [31].

$$w\left(x,y,t\right)=\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\varphi_{mn}\left(x,y\right)q_{mn}\left(t\right) \tag{4}$$

$$\begin{aligned} w(t)=\rho\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\varphi_{mn}(x,y)\,\underset{mn}{\ddot{q}}(t) \\ +c\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\varphi_{mn}(x,y)\,\underset{mn}{q'}(t) \\ +Dq\left(\frac{\partial^4\varphi mn}{\partial x^4}+2\frac{\partial^2\varphi mn}{\partial x^2\partial y^2}+\frac{\partial^4\varphi mn}{\partial y^4}\right) \end{aligned} \tag{5}$$

The ABAQUS package for the FEM analysis was used. The solder connections for a MOSFET can be seen in figure 2. For the simulation, around 120000 nodes and 78000 elements were used for the interconnection modeling of this device. For the solders, the SAC type of Li-free material was used. In order to evaluate the natural frequency and dynamic characteristics of the power MOSFET, the presented method in [29]

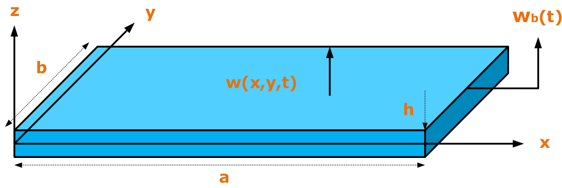

FIGURE 1. Thin rectangular plate.

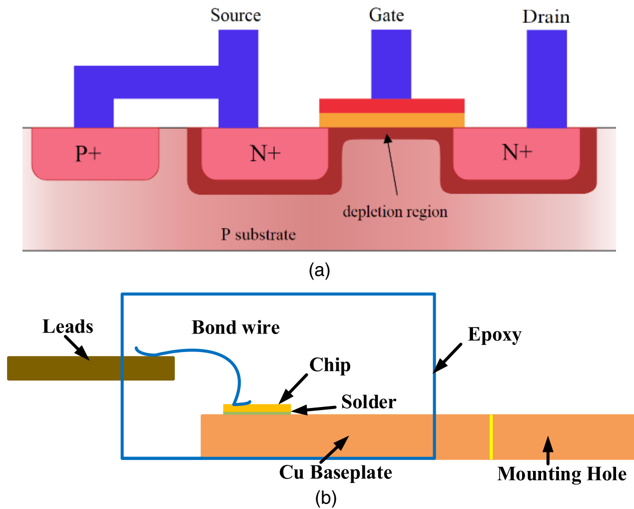

FIGURE 2. (a) Standard MOSFET structure with the depletion regions and (b) Structure of sample discrete power devices.

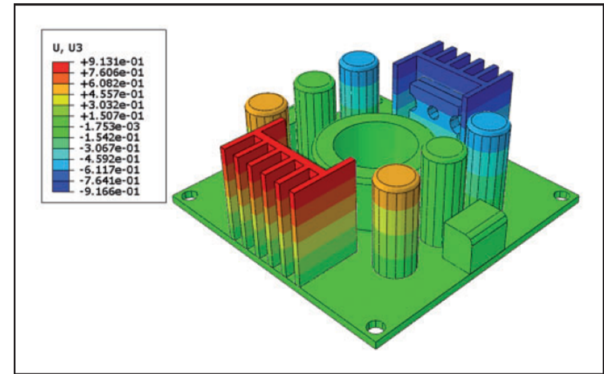

FIGURE 3. Fundamental frequency for the DC-DC boost converter.

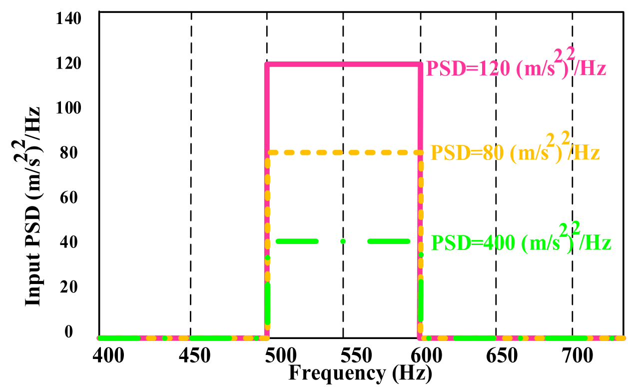

FIGURE 4. Power Spectrum Density (PSD) function versus Frequency.

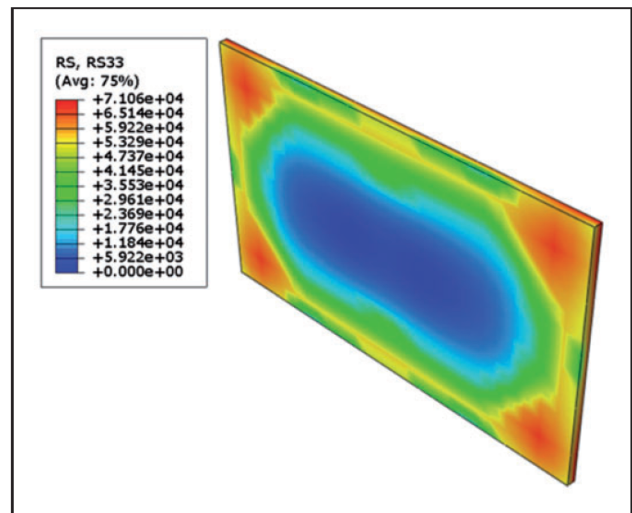

FIGURE 5. A solder layer with the Root-Mean-Square contour of peeling stress.

was used. Based on the results, the fundamental frequency for this device is obtained at around 550 Hz. Figure 3 shows this frequency band. The method is analyzing the mechanical behavior of the narrow bandwidth including the fundamental frequency. The Power Spectrum Density (PSD) function was synchronized with the input vibration. This function is an instrument to Show the average power value of the random input versus the frequency. The used PSD function has been illustrated in figure 4.

This figure shows the PSD in the Root-Mean-Square (RMS) domain according to the frequency. The frequency band is chosen in a way that includes the natural frequency. Figure 5 illustrates the Root-Mean-Square contour of peeling stress in the solder layers. This figure easily can show that the maximum value for the peeling stress can be seen at the corners of the assembled layers. So, as a result, the crack initiations and expansions can be estimated in these locations on the board. This can prove that fatigue failure mostly is affected by the vibration at the corner sides of the electronic board. References [30]–[34] can show us several implemented prototypes that all Show the correctness of our results.

Figure 6 presents the Maximum Peeling (MPa) stress based on the vibration frequency for different PSD inputs. This figure shows that for frequencies **more** than the natural frequency, the RMS value of the MPa dramatically increases and for the higher PSD values the MPa is more. So, the higher PSD values can decrease fatigue life and shorten the useful long-life of the solder layer.

Miner rule is commonly used to estimate the failure rate for the solder joints. For this purpose, normally the equation

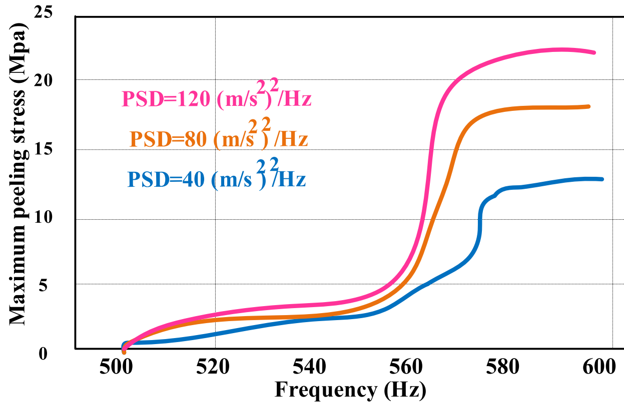

FIGURE 6. MPa versus frequency including the natural frequency.

(6) is presented to show the number of the cycles [31]:

$$D = \int_{0}^{+\infty} \frac{n_S}{N_S} dS = \int_{0}^{+\infty} \frac{N_P(S)}{N_S} dS \tag{6}$$

In this equation, n_S, N_S, and $N_P(S)$ are the numbers of the cycles, mechanical cycles, and cycles to failure respectively. The value of the D based on literature normally is fixed around 0.7 for microelectronics elements. The probability of the density function is defined by:

$$p(S) = \frac{S}{\sigma^2} \exp(-\frac{S^2}{2\sigma^2}) \tag{7}$$

σ in some literature is shown as the S_{RMS} and indicates the standard deviation of random vibration. The fatigue-life can be presented by [32]:

$$S^k N_S = B \tag{8}$$

The values of the k and S are defined by failure tests and are constants. B is the material constant and is defined by fatigue tests. The whole number of cycles to lead the solder-failure is shown by:

$$N = \frac{0.7B}{(\sqrt{2}\sigma)^k \Gamma(\frac{k}{2} + 1)} \tag{9}$$

For the different amounts of the PSDs, by the likelihood-estimator, the values of the coefficients k and B can be defined. For the PSD equal to 40, 80 and 120, the value of the parameter k, will be calculated as 2.52, 2,9 and 3.43 respectively. This can be shown as:

$$S^{2.52} N_S = 0.019 \times 10^{10} \tag{10}$$

$$S^{2.9} N_S = 0.01986 \times 10^{10} \tag{11}$$

$$S^{3.43} N_S = 0.02051 \times 10^{10} \tag{12}$$

B. TC SIMULATION

Figure 7 presents the S (according to MPa unit) diagram versus the number of cycles (S-N) for different PSD input values. This figure proves that for the less number of cycles, the reliability and long-life of the layers are high and close to infinity and higher PSD inputs lead to shorter failure-time. For example, the number of the cycles for the S = 4, under PSD inputs 120, 80 and 40 are around 4×10^6, 6×10^6 and 7.8×10^6 respectively.

For this assessment, the totally around 98000 nodes and 55500 elements are considered for the meshes of the proposed MOSFET. The presented method in [35] is considered to the TC acceleration simulation. A wide range of the temperature is considered from −40 to +130 degrees centigrade for this purpose. This can be followed by figure 8.

For both heat and cool stages, around 8.20°C for the ramp rate is considered. During the TC, constrictions, and expansions are estimated for sharp differences in the TC coefficients. Under the TC, the most common model for TC tests is the Garofalo–Arrhenius (GA) method for the estimation of elastic strains in the joint points. Based on this model, the creep stain $\varepsilon^{\bullet}_{cr}$, for the steady-state condition can be obtained from [32]:

$$\dot{\varepsilon}_{cr} = C_1 [\sinh(C_2\sigma)]^{C_3} \exp^{\frac{-C_4}{T}} \tag{13}$$

In the continuation of the subject, the effects of the Thermal Cycling (TC) is analyzed.

C_1 to C_4 are the constants for the solders based on Sb-material. For the next step, the energy life estimation should be done. The results of the elastic strain for the creep method should be applied for this step. Equation (14) presents the cycles numbers to failure in the solder joints:

$$N_f = (C * .\varepsilon_{acc}) \tag{14}$$

In this equation, N_f, C and ε_{acc} are the number of thermal cycles, creep ductility and deposited creep strain respectively. Figures 9a, 9b and 9c present the stress, accumulated strain and energy of strain under TC for the prototype solder layer.

This figure shows that the stress and strain for the solder layer are maximum at the corners and these parameters values decrease when it approaches the center from the corners. This result confirms other studies like [8], [35]–[38] and shows that the cracks normally start from corners and then spread into the solder joints located at the corners.

Figure 10 illustrates the Finite Element Analysis results and the relation between accumulated creep strain and thermal cycling. According to this figure, by increasing the number of the TC, the accumulated creep strain increases. It indicated that for the low amounts of the TC, a sharp rise appears in the accumulated creep value and.

Although this increment for the accumulated strain continues, the rate of rising is smaller for higher thermal cycling. Also, figure 11 indicates the relation between Von-mises stress and the number of thermal cycling for the proposed module. This figure shows that the amount of stress can be divided into five different classes.

For classes 1 and 2, stress is going to decrease and in class 3 it reaches the minimum value. After that, the stress is increasing again to reach the maximum value. These steps can be seen as classes 4 and 5.

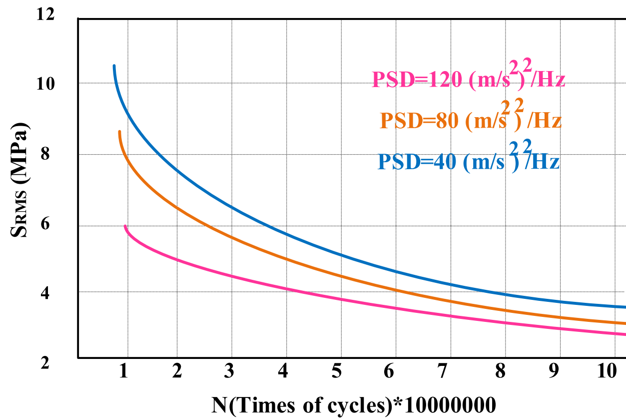

FIGURE 7. S-N curve for different PSD inputs.

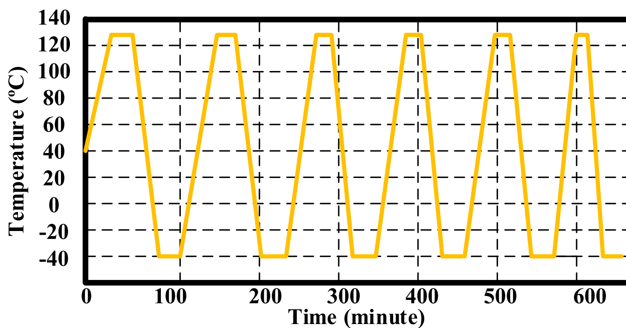

FIGURE 8. TC specifications.

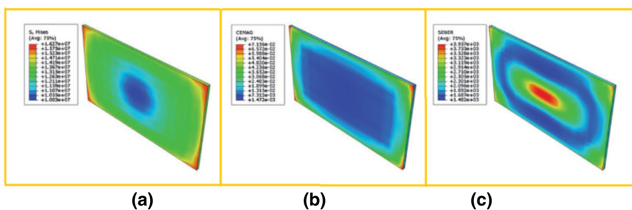

FIGURE 9. The layout of the (a) stress, (b) strain and (c) energy of the strain for the layer.

Classes 1 and 2 is depended on the heating process of the solder layer. It can be interpreted as the first energizing the layer and so the stress is relaxed. This can be continued to the extent that the layer reaches the peak value of the heating. This can be seen as class 3 in figure 11.

This is related to the serious differences between the thermal expansion coefficients between the interconnection of the solder joints and the electronics component. For a comparison between class 1 and 2 in figure 11, it can be seen that at the specified thermal cycling value, the stress will be changed from the relax stage and as the result, the change of the speed for the relax mode of the stress is less after this point for the phase 2 rather than phase 1.

The hot-dwell-time step is synchronized with phase 3 in this curve. This is a critical point and it can be seen that the stage of the stress increment begins in this phase. Factors

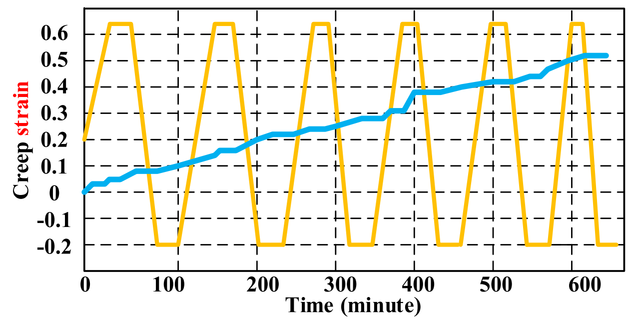

FIGURE 10. Creep strain based on TC.

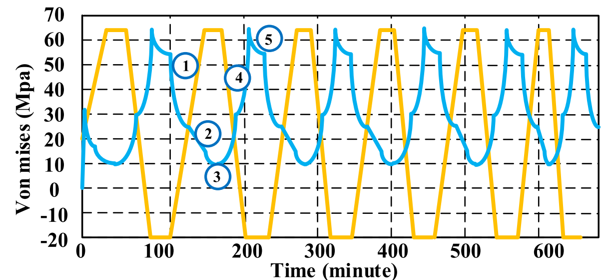

FIGURE 11. Von Mises stress based on TC.

like temperature and stress are the most important parameters for the creep based on FEM results. After the heating stage, the cooling stage begins at the endpoint of phase 3. This phase that can be seen as phase 4 in this figure, is the most important stage for the serious stress changes for the solder layer that is the main factor for the solder fatigue lifetime. At the cooling dwell time in phase 5, the rate of the stress is relaxed in the solder.

After the Von-mises analysis based on the Accumulated Creep Strain (ACS), the fatigue time life for the solder layers is investigated. Results in figure 9 show that for the per cycle ACS value is around 0.060. Based on (14), around 4800 thermal cycling needs for the failure of the proposed solder layer.

III. COMBINATION OF THE RV AND TC, ANALYSIS AND RESULTS

Our general approach to estimating the RV and TC effects on the solder joints can be seen in figure 12. This can be seen that the Root-Mean-Square value of the peeling stress for the RV and accumulated creep strain caused by TC are separately analyzed based on superposition approaches because the types of these effects are independent. The main parameter that caused by the RV is the RMS value of the maximum peeling stress and as this figure shows and mentioned in section II B, for the failure estimation bay the TC effects, the accumulated creep strain or this parameter's energy density should be considered. Based on equation (14) these parameters are used to estimate the number of thermal cycling to failure.

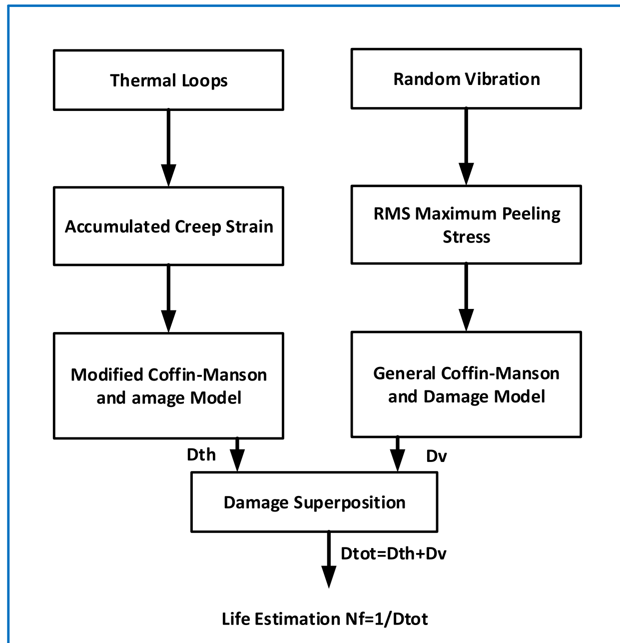

FIGURE 12. Life estimation under the RV and TC effects for the solder layer in a MOSFET interconnection.

Generally, the definitive models that have been presented in the literature for the damage modeling, can be divided into linear and non-linear cumulative approaches. The simplicity, applicability, and accuracy are the main reasons for the selection of these models. The Palmgren-Miner failure approach is one of the common methods that include all of these parameters [32]. Based on this model, DRV and DTC, the damages based on RV and TC can be presented by [32]:

$$D_{RV} = \frac{1}{N_S} \tag{15}$$

$$D_{TC} = \sum_{i=1}^{n} \frac{n_i}{N_{fi}} \tag{16}$$

Figure 13 illustrates the normalized total damage for the proposed MOSFET under both RV and TC effects. Based on this figure's results, under only the thermal loading, the damage is around 0.4. Also, for the vibration under the PSD input equal to 40, the normalized damage is calculated around 0.03.

By higher amounts of the PSD, the damage increases exponentially until that point that for the PSD equal to 120, the damage increases to 0.6. The reason is the deformation at the interconnection point for the solder joint and PCB. Based on this figure, in the worst condition with the thermal loading and 120 PSD as the input vibration, the total damage reaches to one unit.

Different studies show that the void crack formation and expansion in the solder is related to the stress density [25]–[27]. This can be spread out along the solder under vibration and especially when the higher PSD inputs apply to the component, the higher damages can be reported.

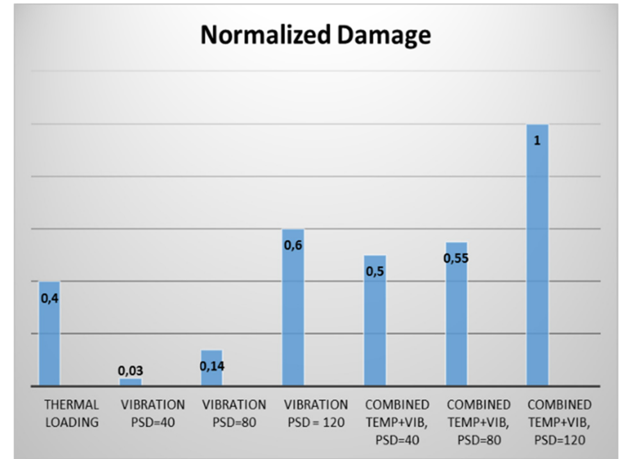

FIGURE 13. Damage estimation under TC and RV.

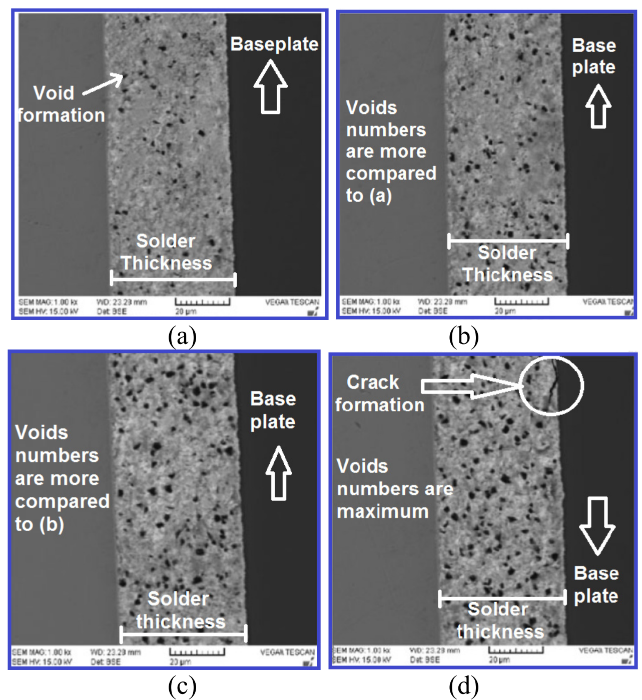

FIGURE 14. Microstructure view of the proposed MOSFET joint under (a) TC, (b) TC and RV with PSD = 40, (c) TC and RV with PSD = 80 and (d) TC and RV with PSD = 120.

Figure 14 presents the and microstructure view of the proposed MOSFET interconnection solder joints with the 34/70 of WTL under a vibration mechanism. These figures are the results of the microscopic observation for the mentioned board under both RV and TC influences with different values of the input PSDs. Figure 14a presents the state of the solder layer under the effect of the thermal cycling. So, as we expected and reported in figure 13, the minimum numbers of the voids are forming. Figure 14b presents the solder joint and interconnection with the baseplate under thermal cycling and random vibration with PSD = 40. This new condition as we expected generate new voids in the solder

layer. Also it was predictable based on figure 13. Also, figure 14c show the same layer and interconnection side under the thermal cycling and higher level of the random vibration (PSD = 80), so as we expected, the number of the voids are increasing for this state. For the last state, in figure 14d, not only the influence of the thermal cycling, but also the effect of the maximum level of the input vibration (PSD =120) is considered. So the numbers of the voids are increasing and crack is formed at the interconnection side of the solder layer and the baseplate. So briefly, figure 14a shows that the voids begin to form under the thermal loops. The voids numbers are increasing under the TC and input PSD equal to 40 as the RV. This can be seen in figure 14b. Figure 14c illustrates the state of the solder layer under the TC and RV equal to 80 PSD. As can be seen the number of voids along with the layer is increased and finally, figure 14d presents the crack formation under both TC and RV with 120 of PSD input. Figure 14d confirms the theoretical analysis presented in this study where the crack is formed at the corner of the layer. This confirms the Finite Element Analysis reports that show the maximum stress and failure occurs in these locations. Vibration frequency is another critical issue for the studied layer behavior analysis. It can be concluded the higher vibration frequencies can accelerate the failure of the solders. As the boundary conditions, the electrical potential, velocity, and electron and lattice temperatures are considered. The electrical potential is considered as the applied voltage constant for the source and drain electrodes and, equal to the electric field constant for the under oxide zone. Also, the temperature is considered based on the lattice temperature for the source and drain pins and zero for the oxide region. Velocity is zero for all electrodes and under oxide region and lattice temperature is closed to zero for oxide zone and source electrode and around the heat transfer value for the drain electrode.

IV. CONCLUSION

In this study, the influences of the Thermal-Cycling (TC) and Random-Vibration (RV) on a MOSFET package are presented separately and simultaneously based on the Finite Element Method Analysis. The accumulated creep stain introduced as the most important parameter of the solder failure for the thermal cycling and the maximum peeling stress presented as the main factor of the fatigue failure for the random vibration. Both RV and TC directly can affect the corners of the solder layers, and crack initiation will form at these locations. The Palmgren-Miner failure approach is considered for combined effects analysis for RV and TC for the MOSFET package. Results show that the higher PSD inputs for the RV and higher TC values can accelerate the speed of formation of the more voids and cause the crack formation at the corner sections of the package. The experimental results confirm the theoretical analysis.

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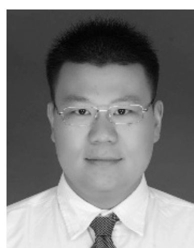

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