Received: 24 February 2020 | Revised: 9 June 2020 | Accepted: 9 July 2020

DOI: 10.1002/2050-7038.12569

RESEARCH ARTICLE

WILEY

A transformer-less single-switch boost converter with high-voltage gain and mitigated-voltage stress applicable for photovoltaic utilizations

Dongping Hu[1] | **Aihua Yin**[1] | **Davood Ghaderi**[2]

[1]School of Software and Internet of Things Engineering, Jiangxi University of Finance and Economics, Nanchang, Jiangxi, China

[2]Electrical and Electronics Engineering Department, Bursa Technical University, Bursa, Turkey

Correspondence
Aihua Yin, School of Software and Internet of Things Engineering, Jiangxi University of Finance and Economics, Nanchang, Jiangxi, China.
Email: xingzuoxng@163.com

Davood Ghaderi, Electrical and Electronics Engineering Department, Bursa Technical University, Bursa, Turkey.
Email: davood.ghaderi@btu.edu.tr

Funding information
The National Natural Science Foundation of China under Grant No. 61702238, No. 61862027, NO.61762043, No. 61661022 and the Science and Technology Foundation of Educational Commission of Jiangxi Province of China under Grant NO. GJJ170316, NO. GJJ180264.

Summary

Many of the photovoltaic (PV) panels generate the low amounts of the voltages under the limited values of the powers. In order to increase these voltages to be applicable for grid utilization, DC-DC boost converters are used. A novel nonisolated transformer-less switched-capacitor-based DC-DC power boost structure is combined with the quadratic converter in this study. The proposed converter has many advantages such the low-voltage stresses on the power components, higher voltage-gain, and ability to supplying the load under the low amounts of the switching time intervals. These features lead to fewer amounts of the currents for the power components in the topology for the continuous conduction mode which means less dynamic losses and higher efficiency. Another advantage of the proposed converter is including only one power switch that simplifies the controller design for implementation purposes. A comprehensive mathematical analysis is presented and simulation with MATLAB/SIMULINK and implemented hardware test results confirm the theoretical investigations.

KEYWORDS

boost converter, continuous current mode, photovoltaic utilizations, switched-capacitor

LIST OF SYMBOLS AND ABBREVIATIONS: CCM, continuous current mode; DT, duty cycle; T, time period; $I_{C2,on}$, currents of capacitors C_2 for the first operation mode; $I_{C3,on}$, currents of capacitor C_3 for the first operation mode; $I_{C4,on}$, currents of capacitor C_4 for the first operation mode; $I_{C5,on}$, currents of capacitor C_5 for the first operation mode; $I_{C2,off}$, currents of capacitor C_2 for the second operation mode; $I_{C3,off}$, currents of capacitor C_3 for the second operation mode; $I_{C4,off}$, currents of capacitor C_4 for the second operation mode; $I_{C5,off}$, currents of capacitor C_5 for the second operation mode; ID1,on, currents of diode D_1 for the first operation mode; ID_2,on, currents of diode D_2 for the first operation mode; ID_3,on, currents of diode D_3 for the first operation mode; ID_4,on, currents of diode D_4 for the first operation mode; ID_5,on, currents of diode D_5 for the first operation mode; ID_6,on, currents of diode D_6 for the first operation mode; ID_1,off, currents of diode D_1 for the second operation mode; ID_2,off, currents of diode D_2 for the second operation mode; ID_3,off, currents of diode D_3 for the second operation mode; ID_4,off, currents of diode D_4 for the second operation mode; ID_5,off, currents of diode D_5 for the second operation mode; ID_6,off, currents of diode D_6 for the second operation mode; ΔiL1, current ripples of the inductor L_1; ΔiL2, current ripples of the inductor L_2; ΔiL3, current ripples of the inductor L_3; ΔVo, voltage ripples of the capacitor C_O; Fs, switching frequency; ΔVc,cap, the ripple value caused by capacitor charging and discharging; P_{VFD}, power losses by diodes.

1 | INTRODUCTION

Efficient, cheap, and reliable switching DC-DC power boost converters are the inevitable intermediate structures for power transmission in renewable energy sources (RESs) especially the photovoltaic (PV) panels and the electrical and electronics industries.[1-3] Since the generated DC voltage of the PV arrays is at a very low level, these converters are applied to increase the voltage before converting to the AC voltage at the grid side.[4,5]

For this reason, various structures have been proposed to increase the voltage. Converters such as conventional boost,[6-9] buck-boost,[10-12] fly-back,[13,14] and Cuk[15,16] have not high-voltage gain, and electromagnetic interference (EMI) and diode back-flow problems can be seen in these converters because the high-voltage gain can be obtained in higher duty cycles for the power switches. Generally, power converters are time-varying nonlinear systems, and due to the uncertainty of the converter parameters, their ability to be accurately modeled in all operating conditions is extremely difficult, so the control process for the power converters is always a major challenge for designers.[17-20] Therefore, normally the single-switched converters based on need only one control block is selected by engineers. The efficiency of the converter is limited by the active power switches, diodes, capacitors, and inductors serial resistances and therefore the cascaded boost converters due to their more components numbers are not recommended.[21,22] In some studies, researchers use an inverter to convert this DC voltage to the AC voltage and in the next step, by a transformer an AC voltage with higher magnitude is obtained for AC utilizations and then by a rectifier block, the desired DC voltage is obtained for DC applications. Although these topologies can obtain the high DC gains, these converters are heavier and more expensive and have lower efficiencies based on the high number of the middle blocks and the components especially the transformer.[23-25] Push-pull, forward and fly-back converters can be categorized in isolated converters that use the transformers and the leakage inductor in the transformer is their second problem. This inductor decreases the efficiency of the converter. For solving these problems, the active-clamp and snubber-based converters are presented, but these converters include high number of components.

Switched-capacitor-based (SC) DC-DC boost converters have been investigated in References 26 to 28. Although, the main purpose of these converters application is to increase the voltage gain and efficiency, many of the SC-cell topologies oblige the power components especially the power switch to endures a high-voltage and current stresses during the transient-time that can directly increase the dynamic losses by considering the internal resistance of the components and decrease the efficiency. Also, normally more than one SC-cell is needed for the high-voltage gain approaches.[26-28]

Various topologies based on the concept of the switched-capacitor cells have been presented in References 26 to 28 in which a soft switching method is used to reduce switching losses and electromagnetic interference problems. Coupled-inductor converters are another solution to improve voltage gain.[29,30] Because in addition to the coefficient of duty, the ratio of the turns of the coupled inductors is another factor in determining the voltage gain. Despite the stated advantage for the coupled inductor type converters, they have a relatively high input current and this can reduce the useful life of the converter input capacitor. Cross-coupled inductors are presented in References 29 and 30 in which an active or inactive clamp circuit is used to achieve soft switching conditions. An interleaved technique is used to reduce the ripple of the input and output components and reduce the size of the capacitors required in the input and output of the converter.[31-34] Applying this technique also reduces the stress of the semiconductor power flow. Interleaved DC-DC converters are presented to decrease the current levels in the converter and the dynamic losses. These topologies, in fact, present a parallel connection of the boost converters which are connected to the same power source and load and the current of the load is dividing between these blocks for more reliability and longer-life time.[33,34] These converters are suitable for high-power applications and for middle levels of the powers, based on the components numbers cannot be reasonable to be applied.

In this study, a novel switched-capacitor cell is presented that can mitigate the voltage stress on drain-source pins of the power switch by making a Snubber configuration and the output voltage is dividing on the switch and SC cell capacitors. The Snubber specification give the ability to prevent high-voltage overshoots on the switch at the start time of the switching. This converter has a high-voltage gain and at the 0.8 of the duty cycle can present a voltage with 70 times greater than the input voltage. The mathematical assessments including the voltage-gain calculations, current for the diodes, capacitors, and inductors, losses investigations and efficiency calculations for the proposed converter is presented in Section 2. Section 3 presents the simulation and experimental results and compares the features of the proposed converter with the several new and well-known topologies for the DC-DC boost converter and Section 4 summarizes the obtained results.

2 | PROPOSED SC-BASED DC-DC BOOST CONVERTER

Figure 1A presents the proposed switched-capacitor-based boost converter. There are three inductors L_1, L_2, and L_3, six capacitors C_1-C_5 and C_O and six diodes D_1-D_6 and one power switch M in this converter. The simplest way to analyze the converter is obtaining the configuration of the converter for the ON and OFF-states of the power switch in two different time intervals for the continuous conduction mode. So, one can obtain the voltage gain of the converter through the KVL and KCL laws.

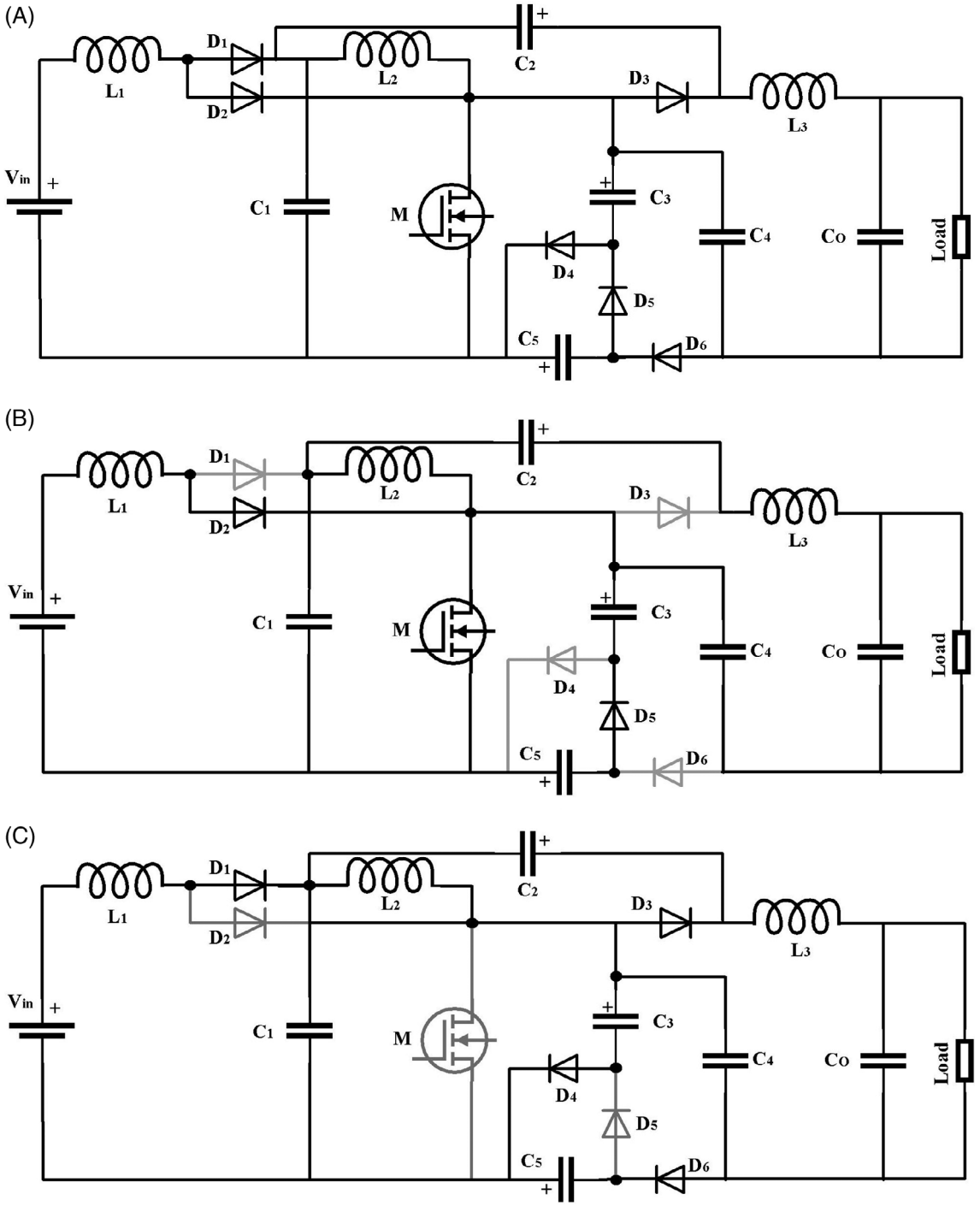


FIGURE 1 A, Proposed switched-capacitor-based boost converter, and the configuration of the converter when the power switch is in, B, ON and C, OFF-states

2.1 | Analysis of the proposed converter in ON and OFF-states of the switch

Figure 1B,C illustrates the configuration of the proposed converter and the connection between components in ON and OFF-states of the switch, respectively.

State 1: As can be seen in Figure 1B, diodes D_2 and D_5 are activated and other diodes are deactivated in this working mode. The maximum voltage on the anode side of the diode D_1 will be equal to zero because the power switch is in short-circuit condition so this diode is deactivated. Also the cathode of this diode is connected to the capacitor C_1 that has a positive voltage and greater than the input voltage. This section of the converter is the input side of the quadratic boost converters that have been analyzed in detail in many researches already.[9,16,35] This voltage will charge the inductor L_2 through the power switch. Figure 2 is presented to give more details for this working state. This figure shows that the voltage across inductors L_1 and L_3 are positive and the currents of these inductors are charging through V_{IN}-D_2-M and L_2-C_2-C_O-C_4 components respectively. The voltage on capacitor C_5 is increasing through the diode D_5. For this, the direction of the current in diode D_5 and polarities of the capacitors should be considered. The orange arrow in Figure 3 shows the path to write the KVL for this loop. The positive polarities of the capacitors are given to better analysis. This loop shows that the voltages of the capacitor C_3 and C_5 are decreasing and increasing in this operational mode. Capacitors C_2 and C_4 are charging the currents of the inductor L_3 and output capacitor C_O. For this loop, the current of the capacitor C_1 also is discharging on inductor L_3 and output capacitor. Loops with purple and green colors show these states. Equations (1) to (4) are written based on loops with blue, orange, red, and green colors, respectively.

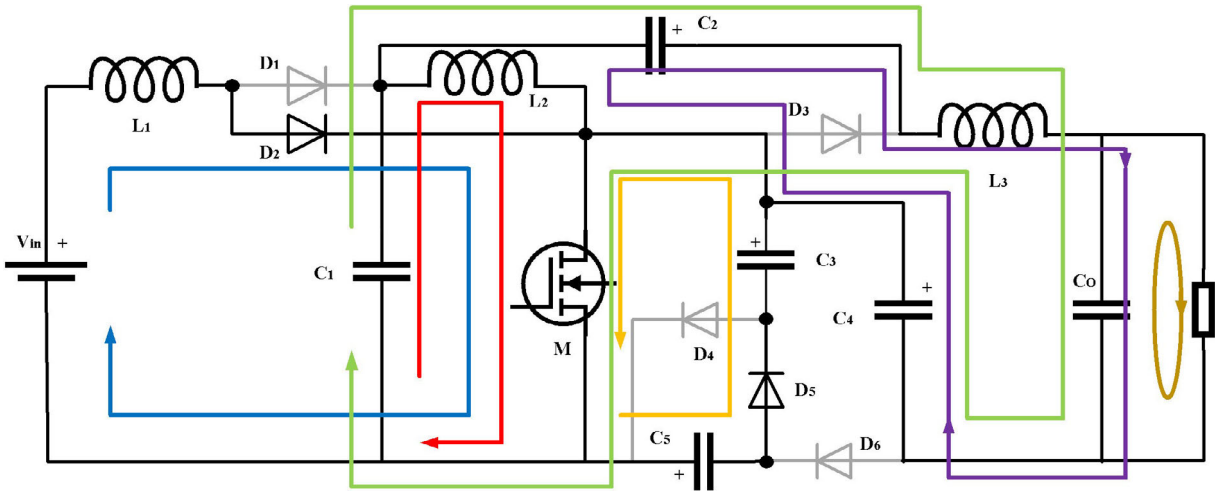


FIGURE 2 State of the components for ON-time interval of the switch and KVL loops

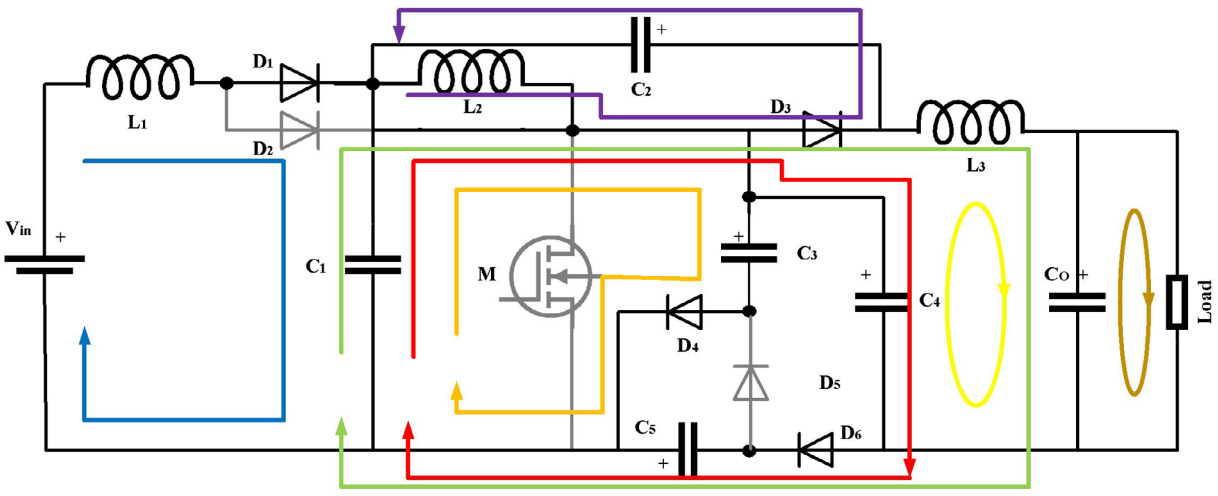


FIGURE 3 State of the components for OFF-time interval of the switch and KVL loops

$$V_{L1} = V_i \tag{1}$$

$$V_{C3} = V_{C5} \tag{2}$$

$$V_{L2} = V_{C1} \tag{3}$$

$$V_{L3} = V_{C1} + V_{C2} + V_{C4} - V_o \tag{4}$$

Voltage at the input and output sides of the converter and across inductors L_1, L_2, and L_3, and capacitors C_1 to C_5 and C_O are presented by V_i and V_O, V_{L1}, V_{L2}, and V_{L3} and V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C5}, and V_{CO}, respectively.

State 2: Unlike the first case, diodes D_2 and D_5 are deactivated in this working mode according to Figures 1C and 3. The voltage across the capacitor C_1 is increasing through the inductor L_1 via the input voltage and because the voltage across this inductor is negative, the current of the inductor begins to decrease. Also, the voltage on the capacitor C_2 is increasing through the inductor L_2 and diode D_3 that can be seen by purple loop color in Figure 3. Voltage of the capacitors C_3 and C_4 are increasing respectively through the diode D_4 and D_6. These states can be tracked by orange and red loops in Figure 3. Also, the state of the capacitor C_5 shows that the voltage of the capacitor is decreasing in this operational mode. By considering the loops with blue, purple, orange and yellow colors simply the Equations (5) to (8) can be obtained as follows:

$$V_{L1} = V_{in} - V_{C1} \tag{5}$$

$$V_{L2} = -V_{C2} \tag{6}$$

$$V_{L2} = V_{C1} - V_{C3} \tag{7}$$

$$V_{L3} = V_{C4} - V_o \tag{8}$$

$$V_{C4} = V_{C3} + V_{C5} \tag{9}$$

Equation (9) shows that the voltage on the capacitor C_4 is equal to the total voltages of the capacitors C_3 and C_5. Figure 4 is presented to show the voltage and current states of the different components in this converter for ON and OFF-time intervals of the power switch. To obtain this figure, the states of the components are considered through Figures 1B,C, 2, and 3.

2.2 | Voltage-gain assessment for the converter

Duty cycle D is a ratio that can present the ON-time duration for the power switch according to a period time T:

$$D = \frac{T_{on}}{T} \tag{10}$$

In this equation T_{on} is the time interval duration that the switch is activated. The average voltage across an inductor is zero in a time period. This is well-known as the voltage-balance theorem.[36] By considering this theorem for the inductor L_2, through Equations (3) and (6) one can write:

$$\int_0^{DT} V_{C1} dt + \int_{DT}^{T} (-V_{C2}) dt = 0 \tag{11}$$

The voltage value for the capacitor C_2 is equal to:

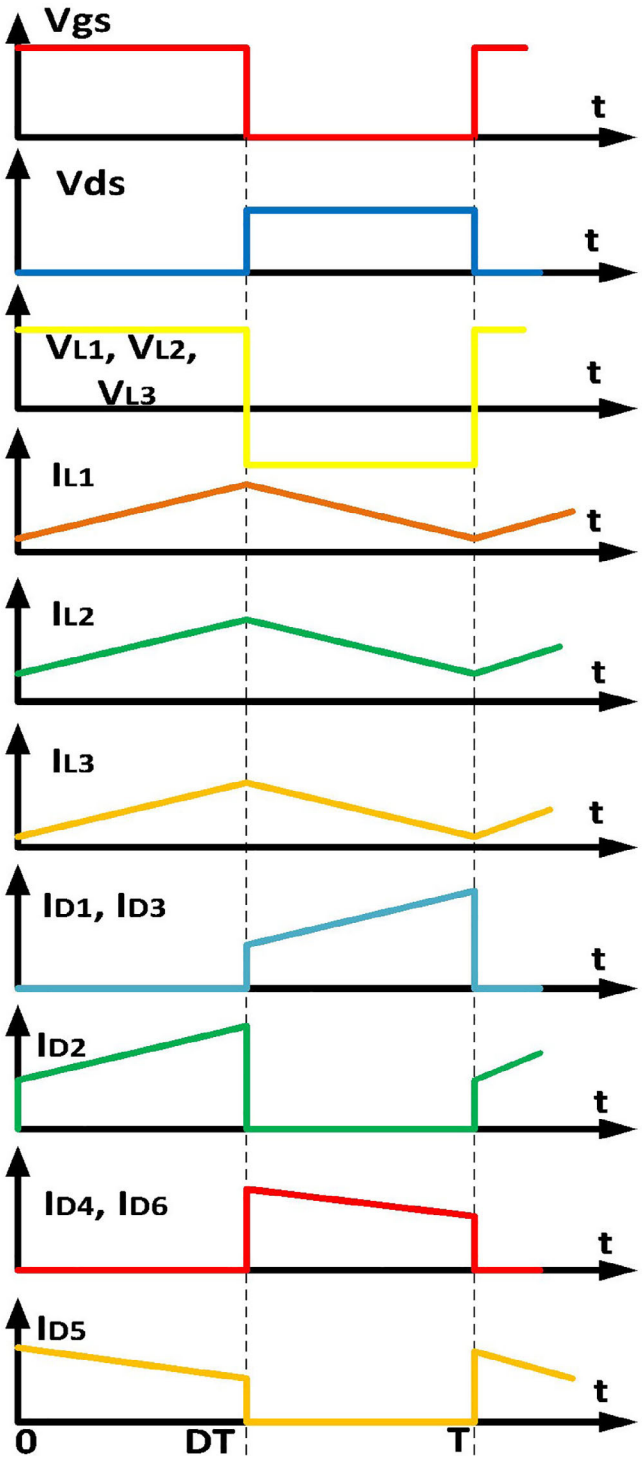


FIGURE 4 The states of the different components under ON and OFF-switching time intervals. Inductors are charged and discharged simultaneously and the diodes D_1, D_3, D_4, and D_5 activated and deactivated simultaneously for these times intervals

$$V_{C2} = \frac{DV_{C1}}{1-D} \tag{12}$$

Also, the voltage across the capacitor C_1 can be obtained as:

$$V_{C1} = \frac{V_i}{1-D} \tag{13}$$

By replacing the Equation (13) into (12), one can write:

$$V_{C2} = \frac{V_i}{(1-D)^2} \tag{14}$$

The same theorem for this inductor can be rewritten through Equations (3) and (7):

$$\int_0^{DT} V_{C1} dt + \int_{DT}^{T} (V_{C1} - V_{C3}) dt = 0 \tag{15}$$

Through the Equation (2), the voltage on capacitors C_3 and C_5 can be obtained as follows:

$$V_{C3} = V_{C5} = \frac{V_{C1}}{1-D} = \frac{V_i}{(1-D)^2} \tag{16}$$

As mentioned for Equation (9), the voltage on capacitor C_4 is equal to the total voltages across the capacitors C_3 and C_5:

$$V_{C4} = \frac{2V_{C1}}{1-D} = \frac{2V_i}{(1-D)^2} \tag{17}$$

The voltage-balance theorem can be written for the inductor L_3 as follows:

$$\int_0^{DT} (V_{C1} + V_{C2} - V_{C3} + V_{C4} + V_{C5} - V_o) dt + \int_{DT}^{T} (V_{C4} - V_o) dt = 0 \tag{18}$$

By replacing the Equations (12) to (17), under the continuous conduction mode, the voltage gain of the proposed converter can be obtained as follows:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2+D}{(1-D)^2} \tag{19}$$

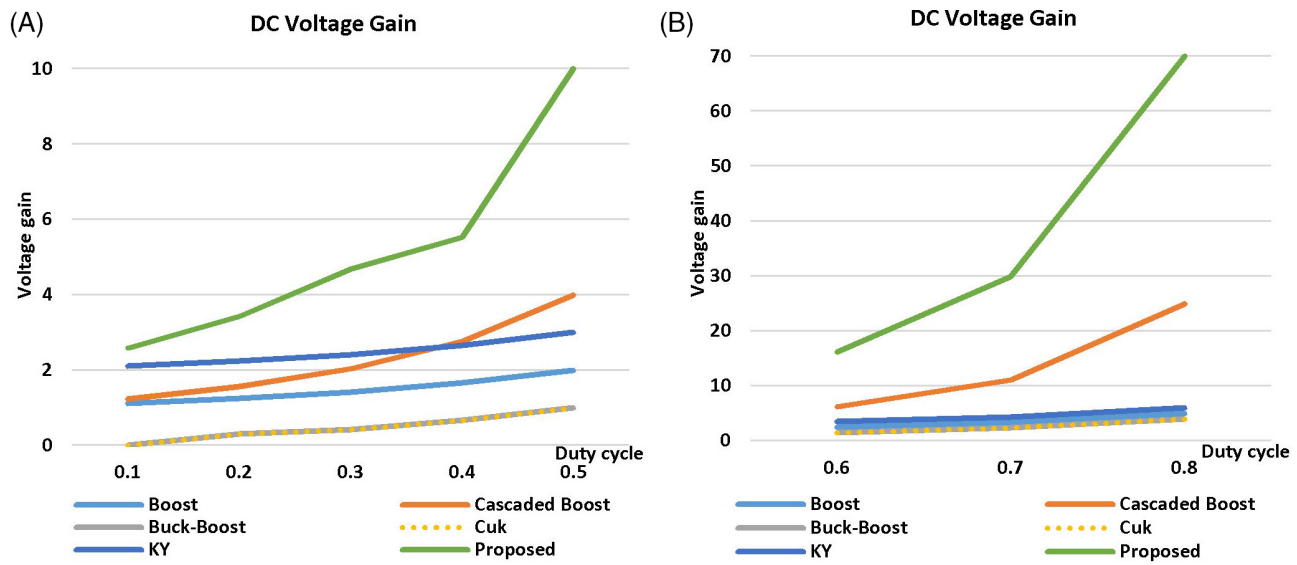


FIGURE 5 The voltage gain of the proposed converter and other conventional boost and buck-boost converters, for the duty cycles, A, $D \leq 0.5$; B, $D \geq 0.5$

Figure 5A,B is presented for the voltage-gain crosscheck of the proposed DC-DC boost converter and the conventional Boost, Buck-Boost, Cuk, Cascaded Boost, and KY Boost converters. This figure easily can prove that the gain of the proposed converter is higher for all different duty ratio values with the comparison for these converters. The reason that gain curves presents in two sub-figures is that presenting a better comparison for voltage-gain that begin from around 0 to around 70 for $0 < D < 0.8$.

2.3 | Components current calculations

According to the state of the components in Figure 1B, the current follows through the capacitors C_2, and C_4 and the inductor L_3 and the load can be presented by Equation (20):

$$-I_{L3} = I_{C2,on} = I_{C4,on} = -I_o \tag{20}$$

$I_{C2,on}$ and $I_{C4,on}$ present the currents of the capacitors C_2 and C_4 for ON-state of the power switch. According to the voltage-balance theorem for the inductors, the current-balance theorem can be presented for the capacitors.[36] Based on this principle, the average current follows through a capacitor in a time period including both ON and OFF-time intervals is equal to zero. At the first step, this theorem can be applied for the capacitor C_4 as follows:

$$\int_0^{DT} I_{C4,on}dt + \int_{DT}^{T} I_{C4,off}dt = 0 \tag{21}$$

$I_{C4,on}$ can be replaced by Equations (20) and (22) can be used to find the $I_{C4,off}$:

$$I_{C5,off} = -\left(I_{L3} + I_{C4,off}\right) \tag{22}$$

These equations also can be used for the current of the capacitor C_5:

$$I_{C5,off} = -\frac{I_o}{1-D} \tag{23}$$

$I_{C5,off}$ presents the current of the capacitor C_5 for the OFF-state operational mode. Since the same current follows through the capacitors C_5 and C_3 but in reverse direction, one can write:

$$I_{C5,on} = -I_{C3,on} = \frac{I_o}{D} \tag{24}$$

$I_{C5,on}$ and $I_{C3,on}$ present the current of the capacitors C_3 and C_5 for ON-state. Equation (24) is written by considering the Figures 1B and 2 and shows the capacitors C_5 and C_3 are charging and discharging through the power switch, respectively. By considering the second operational mode, the current of the inductor L_2 can be written as follows:

$$I_{L2} = I_{C2,off} + I_{C3,off} + I_{C4,off} + I_{L3} = \frac{2+D}{1-D}I_o \tag{25}$$

$I_{C2,off}$, $I_{C3,off}$, *and* $I_{C4,off}$ present the currents of the capacitors C_2, C_3, and C_4, respectively. The current equations for the power diodes D_3, D_4, D_5, and D_6 will be obtained through Equations (26) to (29), respectively:

$$I_{D3} = I_{C2,off} + I_{L3} = \frac{I_o}{1-D} \tag{26}$$

$$I_{D4} = I_{C3,off} = \frac{I_o}{1-D} \tag{27}$$

$$I_{D5} = -I_{C3,on} = \frac{I_o}{D} \tag{28}$$

$$I_{D6} = -I_{C5,off} = \frac{I_o}{1-D} \tag{29}$$

I_{L2}, $I_{C2,on}$, *and* $I_{C4,on}$ are parameters that will be specify the current of the power switch:

$$I_M = I_{L2} - I_{C2,on} - I_{C4,on} = \frac{1+2D}{D(1-D)} I_o = \frac{V_o^3 - V_o V_{C1}^2}{\left(V_{C1} V_o - 2V_{C1}^2\right) R} \tag{30}$$

By replacing the Equation (13) for the voltage of the capacitor C_1 into Equation (30), this current is obtained as follows:

$$I_M = \frac{V_o^3 - V_o V_{C1}^2}{\left(V_{C1} V_o - 2V_{C1}^2\right) R} = \frac{V_o^3 - V_o \frac{V_i}{(1-D)^2}}{\left(\left(\frac{V_i}{1-D}\right) V_o - 2\frac{V_i^2}{(1-D)^2}\right) R} \tag{31}$$

The current of the input source side, by considering the ON and OFF-states of the switch and configurations presented in Figures 1B,C, 2, and 3, can be written by Equation (32):

$$I_i = \int_0^{DT} (I_{L2} - I_{C2,on}) dt + \int_{DT}^{T} \left(I_{L2} - I_{C2,off}\right) dt = \frac{2+D}{(1-D)^2} I_o \tag{32}$$

This equation presents the relation between input current I_i and output current I_O.

2.4 | Inductor current ripples calculation

The current ripples for the inductors of the proposed converter generally can be obtained as follows:

$$\Delta I_L = \frac{D V_i}{L f_s} = \frac{D(1-D) V_o}{(2+D) L f_s} = \frac{V_i V_o - 2V_i^2}{(V_i + V_o) L f_s} \tag{33}$$

ΔI_L, L, and f_s present the ripple value for the current of the inductor, related inductor and switching frequency of the converter respectively. By this equation, the maximum ripple value $\Delta I_{L,max}$ can be calculated in term of the minimum level of the duty cycle D_{min}:

$$\Delta I_{L,max} = \frac{D_{min} V_{i,max}}{L f_s} = \frac{D_{min}(1-D_{min}) V_o}{(2+D_{min}) L f_s} \tag{34}$$

So if $I_{L,av}$ presents the average current of the inductors, the maximum current can be obtained for the inductors L_1, L_2, and L_3 through Equations (35) to (37):

$$I_{L1,max} = I_{L1,av} + \frac{\Delta I_{L1}}{2} = \frac{2+D}{(1-D)^2} I_o + \frac{D(1-D) V_o}{2(2+D) L_1 f_s} \tag{35}$$

$$I_{L1,max} = I_{L1,av} + \frac{\Delta I_{L1}}{2} = \frac{2+D}{1-D} I_o + \frac{\mathrm{D}(1-D)V_o}{2(2+D)L_1 f_s} \tag{36}$$

$$I_{L2,max} = I_{L2,av} + \frac{\Delta I_{L2}}{2} = I_o + \frac{D(1-D)V_o}{2(2+D)L_2 f_s} \tag{37}$$

2.5 | Ripples calculations for the output capacitor

This ripple ΔV_o can be obtained through the classic equation of the electrical charge ΔQ for the capacitor that is presented as (38):

$$\Delta V_o = \frac{\Delta Q}{C_o} = \frac{1}{C_o} \times \frac{\Delta I_{L3}}{2} \times \frac{T_s}{2} \times \frac{1}{2} = \frac{V_o D(1-D)}{8(2+D)L_3 C_o f_s^2} \tag{38}$$

This equation is presented to find the minimum value of the output capacitor $C_{o,min}$ to fix the output voltage at the desired level:

$$C_{\mathrm{o},min} = \frac{\Delta I_{L3,max}}{8 f_s \Delta V_o} = \frac{V_o D_{\min}(1-D_{\min})}{8(2+D_{\min})L_3 f_s^2 \Delta V_o} \tag{39}$$

2.6 | Efficiency calculations

The efficiency of the converter can be obtained by considering of the internal resistance for the circuit components. This resistance for the power switch in ON-state is shown by r_{DS}, for diodes are shown by P_{RF1} to P_{RF6}, for capacitors by R_{C1} to R_{C5} and R_{CO} and for the inductors by $r_{L1}$to r_{L3}. The threshold voltage for the diodes can be shown by V_{F1} to V_{F6}. The dynamic losses can be calculated by the effective value of the switch current. This current $I_{S,rms}$, can be written by (47):

$$I_{S,rms} = \sqrt{\frac{1}{T}\int_0^{DT} (I_{L2} - I_{C3,on} - I_{C4,on})^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{1+2D}{D(1-D)} I_o\right)^2 dt} = \frac{1+2D}{\sqrt{D}(1-D)} I_o \tag{40}$$

So, the dynamic losses for the switch will be equal to:

$$P_{rDS} = r_{DS} I_{S,rms}^2 = r_{DS} \frac{(1+2D)^2}{D(1-D)^2} I_o^2 \tag{41}$$

The switching losses of this switch can be written as:

$$P_{Sw} = f_s C_S V_S^2 = f_s C_S \left(\frac{V_{C1}}{1-D}\right)^2 = f_s C_S \frac{V_i^2}{(1-D)^2} \tag{42}$$

In (42), C_S and V_S are the output capacitor of switch and the voltage on switch when is deactivated respectively. Equation (42) can be rewritten as:

$$P_{SW} = f_s C_S \left(\frac{(M_{CCM} + 2) V_o}{4 M_{CCM}} \right)^2 \tag{43}$$

So, the total losses for the power switch can be obtained as follows:

$$P_{Switch} = P_{rDS} + \frac{P_{Sw}}{2} \tag{44}$$

The effective current for the Diodes D_1 and D_2 can be calculated:

$$I_{D1,rms} = \sqrt{\frac{1}{T} \int_{DT}^{T} \left(\frac{I_o}{1-D} \right)^2 dt} = \frac{I_o}{\sqrt{1-D}} \tag{45}$$

$$I_{D2,rms} = \sqrt{\frac{1}{T} \int_{0}^{DT} \left(\frac{(2+D) I_o}{1-D} \right)^2 dt} = \frac{(2+D) I_o}{1-D} \sqrt{D} \tag{46}$$

The dynamic losses of diodes can be obtained by (47):

$$(P_{RF})_D = R_F I_{D,rms}^2 \tag{47}$$

The average values for the currents of the diodes $I_{D1,av}$ should be considered for calculation for the losses on these diodes when are activated.

So, the losses on these diodes when are activated can be shown by:

$$(P_{VF})_D = V_F I_{D,av} \tag{48}$$

Also, for the capacitors, the effective current values $I_{C,rms}$ should be considered to obtain the power losses on these components. In Equation (49), r_C is the serial equivalent resistance for the capacitors:

$$P_{RC} = r_C I_{C,\mathrm{rms}}^2 \tag{49}$$

The effective current values $I_{L,rms}$ for the inductors L_1, L_2, and L_3 and the power losses on these inductors P_{rL} can be calculated through Equations (50) to (52), respectively:

$$I_{L1,rms} = \left(\frac{2+D}{1-D} \right)^2 I_o \rightarrow P_{rL1} = R_{L1} I_{L1,rms}^2 = R_{L1} \left(\frac{2+D}{1-D} \right)^2 I_o^2 \tag{50}$$

$$I_{L2,rms} = \frac{2+D}{1-D} I_o \rightarrow P_{rL2} = R_{L2} I_{L2,rms}^2 = R_{L2} \left(\frac{2+D}{1-D} \right)^2 I_o^2 \tag{51}$$

$$I_{L3,rms} = I_o \rightarrow P_{rL3} = R_{L3} I_{L3,rms}^2 = R_{L3} I_o^2 \tag{52}$$

So the total losses for all components can be calculated by:

$$P_{loss} = P_M + \sum_{a=1}^{6} (P_{RF})_{Da} + \sum_{u=1}^{6} (P_{VF})_{Da} + \sum_{a=1}^{6} P_{RCa} + P_{rL1} + P_{rL2} + P_{rL3} + P_{RCo} \tag{53}$$

The efficiency equation for the converter can be obtained generally by:

$$\eta = \frac{P_o}{P_o - P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P_o}} \tag{54}$$

By replacing the Equation (53) into Equation (54), efficiency for the proposed converter can be obtained as follows:

$$\eta = \frac{1}{1 + \frac{\varphi}{RD(1-D)^2} + r_{Co}\frac{D^2(1-D)^2R}{12(2+D)^2L_3^2f_s^2} + \frac{f_sC_sV_i^2}{(1-D)^2RI_o^2}} \tag{55}$$

In Equation (55), φ can be summarized by (56):

$$\begin{aligned}\varphi = (1+2D)^2 r_{DS} + D(1-D)(R_{F3}+R_{F4}+R_{F6}) + \frac{D(1-D)^2}{I_o}\sum_{u=1}^{6} V_{Fu} + (1-D)^2R_{F5} + D^2(1-D)(r_{C2}+r_{C4}) \\ + (1-D)(r_{C3}+r_{C5}) + DR_{L1} + (2+D)^2DR_{L2} + D(1-D)^2R_{L3}\end{aligned} \tag{56}$$

Also, the voltage stress on the drain-source pins of the power switch is equal to:

$$V_S = \frac{V_{C1}}{1-D} = \frac{Vo}{(1-D)^2} \tag{57}$$

Based on the Equation (57), the voltage stress across the switch is less than the output voltage and the output voltage is dividing on the switched-capacitor cell block components to impose the less amount of voltage on the switch. This increases the reliability and long-life of the converter and decreases the losses of the switch.

2.7 | The voltage ripples of the capacitors

Figure 6A presents the estimated ripple curve for the capacitor C_2. The ripple amplitude is shown with ΔV_{C2}. $\Delta V_{C2,ESR}$ is the ripple value caused by equivalent serial resistance of C_2 and $\Delta V_{C2,cap}$ is the ripple value caused by charging and discharging of this capacitor. The actual voltage across the capacitor is in form of the curve indicated in red color in this figure. The orange curve has been given to present the impact of the ΔV_C, $\Delta V_{C,cap}$, and $\Delta V_{C,ESR}$ components on the voltage. So, the ripple for this capacitor can be obtained from:

$$\Delta V_{C2} = \Delta V_{C2,ESR} + \Delta V_{C2,cap} \tag{58}$$

The maximum ripple value is equal to:

$$\Delta V_{C2,ESR} = ESR_{C2}\Delta I_{C2} \cong ESR_{C2}\left(I_{C2,off} - I_{C2,on}\right) = \frac{ESR_{C2}I_o}{1-D} \tag{59}$$

In this equation, ESR_{C2} is defined by:

$$ESR_{C2} = \frac{tan\delta_{C2}}{2\pi f_s} \tag{60}$$

That, $tan\delta_{C2}$ is the losses coefficients of this capacitor. $\Delta V_{C2,cap}$ can be presented by:

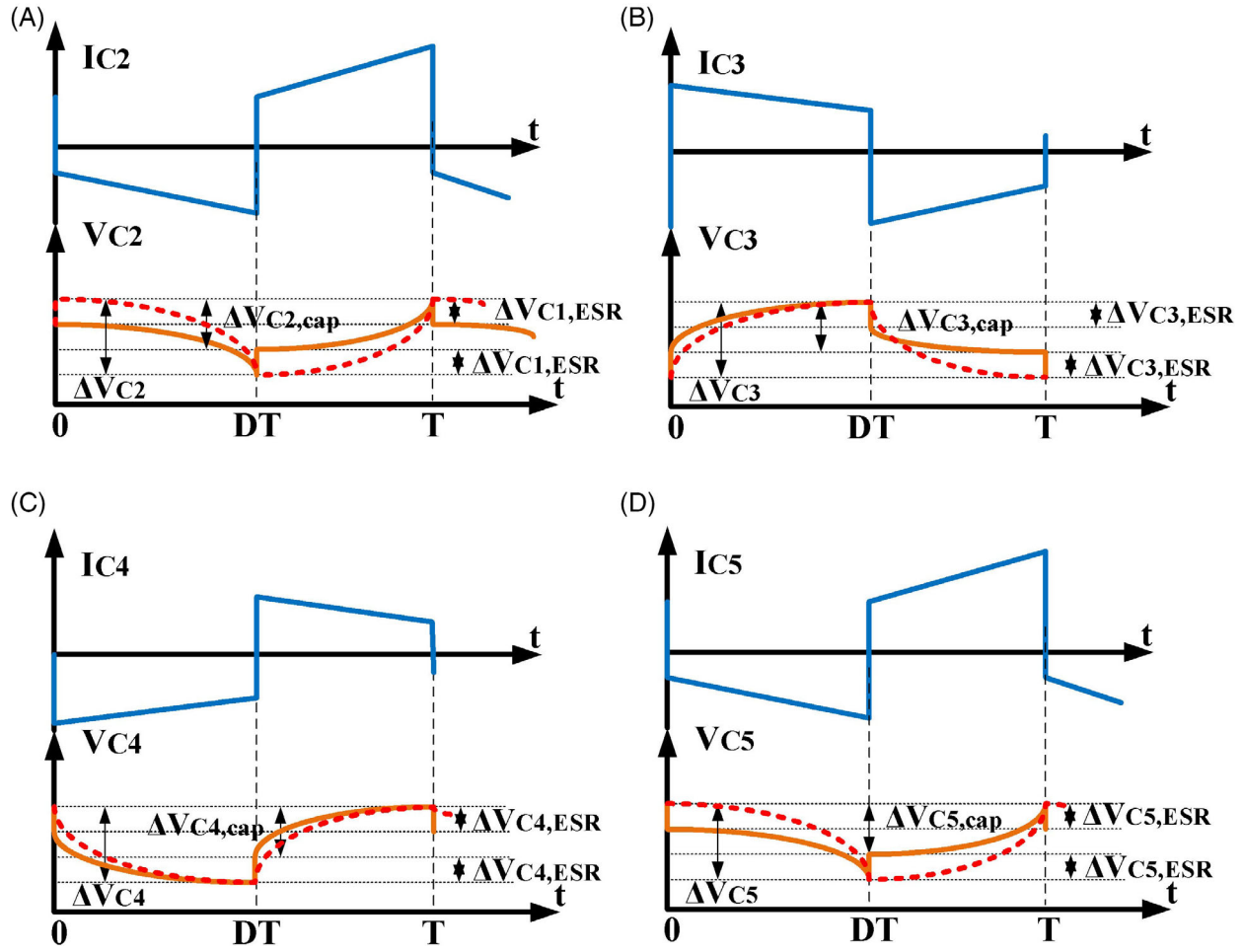


FIGURE 6 Voltage and current waveforms for capacitors, A, C_2; B, C_3; C, C_4; and D, C_5

$$\Delta V_{C2,cap} = \frac{I_{C2,off}(1-D)T}{C_2} = \frac{DTV_o}{RC_2} \tag{61}$$

The same fact can be presented for the capacitors C_3, C_4, and C_5. The current and voltage curves for these capacitors are illustrated in Figure 6B-D, respectively. In Equations (62) to (66), $\Delta V_{C,ESR}$ is the ripple value caused by equivalent serial resistance of capacitors and $\Delta V_{C,cap}$ is the ripple value caused by charging and discharging of the capacitors. So, the ripple for the capacitors C_3, C_4, and C_5 can be obtained respectively from:

$$\Delta V_{C3,4,5} = \Delta V_{C3,4,5ESR} + \Delta V_{C3,4,5cap} \tag{62}$$

$$\Delta V_{C3,4,5ESR} = ESR_{C3,4,5}\Delta I_{C3,4,5} \cong ESR_{C3,4,5}\left(I_{C3,4,5,on} - I_{C3,4,5,off}\right) = \frac{ESR_{C3,4,5}I_o}{D(1-D)} \tag{63}$$

$$ESR_{C3,4,5} = \frac{tan\delta_{C3,4,5}}{2\pi f_s} \tag{64}$$

$$\Delta V_{C3,4,5cap} = \frac{I_{C3,4,5on}DT}{C_{3,4,5}} = \frac{TV_o}{RC_{3,4,5}} \tag{65}$$

The voltage ripple for the output capacitor is defined by:

$$\Delta V_o = \frac{V_o D(1-D)}{8(2+D)L_2 C_a f_s^2} \tag{66}$$

A comparison has been done to evaluate the performance of the proposed converter with some of the well-known DC-DC boost structures. Table 1 presents this comparison. The proposed converter is including the more inductors, diodes, and capacitors and has only one power switch that is less than the number of switches for the proposed converters in References 37 and 38. The main advantages of the projected topology can be summarized in high-voltage gain and mitigated-voltage stress features on the main power switch. These two important parameters are compared in Table 1 and for better understanding, Figure 7 is presented. Figure 7A,B shows this comparison separately for the voltage gain and voltage stress.

Since the converters in References 39 and 40 have the (1-2D) term in the denominator of their gain equation, so the duty cycles equal or near to 0.5 are the critical switching ratios for these structures, and switching should be avoided in this area. Switching with these duty cycles endures high-voltage stress near to output voltage on the power components especially across the power switch that causes serious damages to the switch and other power elements and an abrupt increment in the circuit losses.

For other amounts of the duty cycles, the voltage gain of the proposed converter shows the best result and the voltage stress is less for this converter for duty cycles more than 0.5. For smaller duty ratios, the generated voltage across the switch is not high enough to damage the switches in all converters presented in References 37–39, and the proposed topology.

TABLE 1 Comparison between proposed and other boost converters

Parameter	37	38	39	40	41	Proposed
Inductors	2	2	2	2	2	3
Capacitors	3	5	3	3	3	6
Diodes	4	4	3	2	2	6
Switches	2	1	2	1	1	1
Voltage gain	$\frac{2}{1-D}$	$\frac{2+D}{1-D}$	$\frac{3+D}{1-D}$	$\frac{1}{1-2D}$	$\frac{2(1-D)}{(1-2D)}$	$\frac{2+D}{(1-D)^2}$
Stress on switches	$\frac{VO}{2}$	$\frac{VO}{2+D}$	$\frac{VO+Vin}{4}$	Vo	$VO - Vin$	$(1-D)^2 Vo$

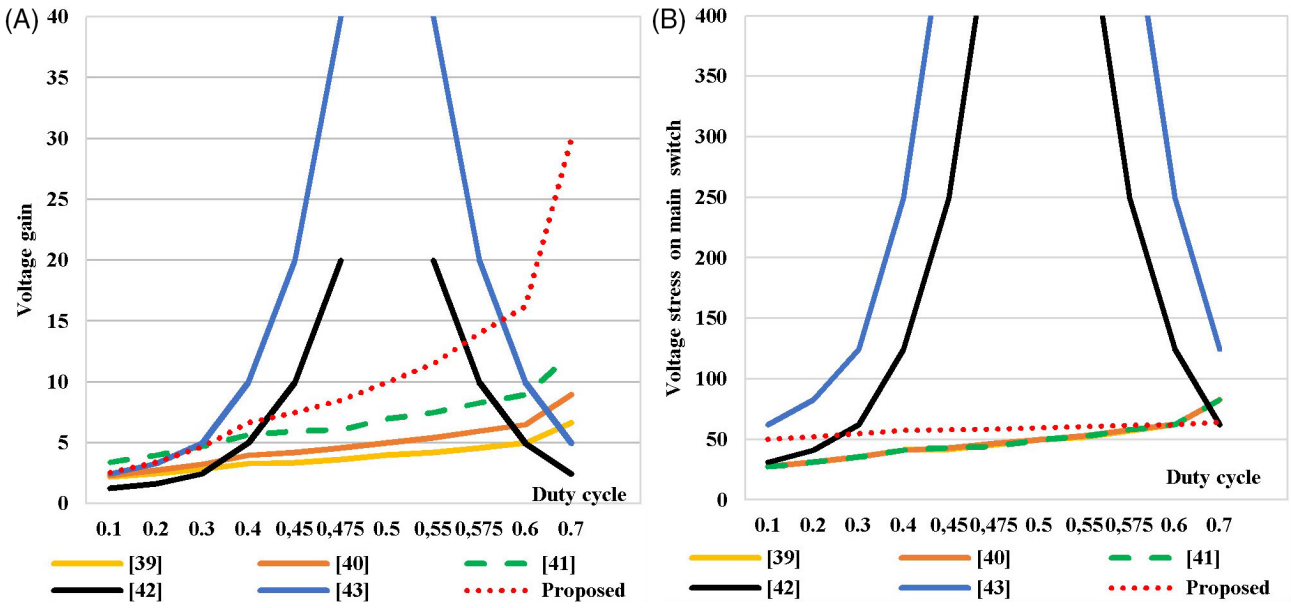


FIGURE 7 A comparison between the proposed and other DC-DC boost converters, A, voltage gain; B, voltage stresses across main power switch

3 | SIMULATION AND EXPERIMENTAL RESULTS

In order to confirm the investigated mathematical analysis for the proposed converter, in this section, the simulation and hardware test results are presented. The components specifications are shown in Table 2. In order to prepare a comparison for the simulation and experimental results, the same values for the components are selected. The power switch is derived under 50% of the duty cycle D = 0.5. Based on Equation (19), for the input voltage equal to 24 V DC, a voltage with around 240 V DC amplitude at the output of the converter is expected.

Figure 8A presents the input and output voltages and shows that the desired voltage has been obtained. Figure 8B illustrated the input and output current for the projected converter.

Based on the Equation (32), and by considering the Table 2 parameters, for the 170 W as the output power, since the output voltage is fixed at the 240 V DC, a current around 0.7 A of magnitude for the load side is expected. So, current with the average amount of 7 A is expected at the input side. Figure 8B shows that that the expected current is obtained in the input side.

In different studies for the design of a power converter including the buck, boost, or buck-boost structures, the design is done in such a way that the magnitude of the ripple of the current flowing through the inductor does not exceed 50% of the average current of the inductor.[36-41] In the proposed converter, since the maximum ripple and average current values are 2A and 7A, respectively, this ratio will be around 28% that is considered as a good design. Also, the Equation (34) shows that the fewer ripples can be obtained for the input current with a greater inductor or higher switching frequency. The main concern is that there is a reverse relation between the frequency and value of the inductor. It means that for the higher frequencies one has to apply a smaller inductor and vice versa. Also, applying a small inductor is not recommended for high-power utilizations including the converter and inverter blocks since the

TABLE 2 Components values

Parameter	Simulation	Experimental
Input voltage	24 V DC	24 V DC
Output voltage	240 V DC	240 V DC
Output power	170 W	170 W
L_1, L_2	200 uH	200 uH
L_3	100 uH	100 uH
C_1	100 uF	100 uF
C_2, C_3, C_4, C_5	100 uF	100 uF
C_O	470 uF	470 uF
D_1-D_6	Based on DSEP15-06A specifications	DSEP15-06A
MOSFET	Based on IXTQ460P2 specifications	IXTQ460P2
Switching frequency	50 KHz	50 KHz

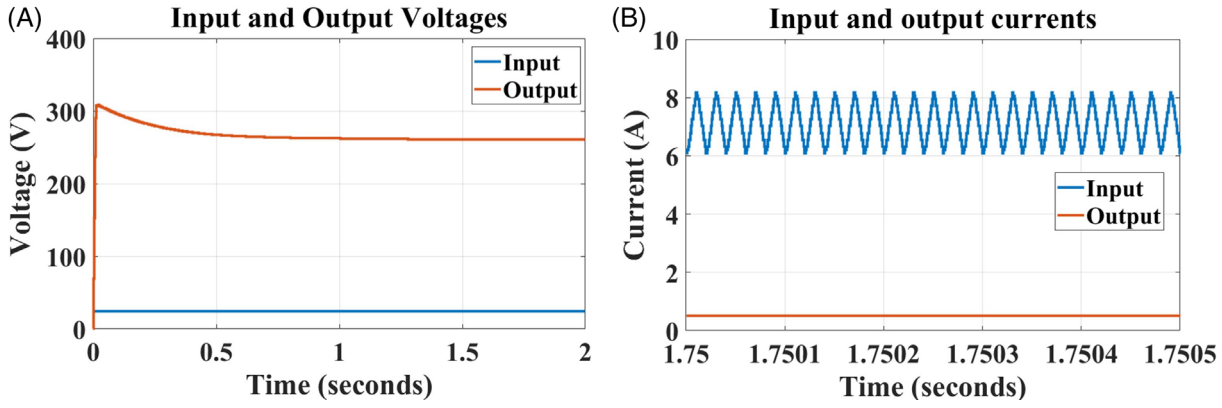


FIGURE 8 The input and output, A, voltage, and B, current waveforms under D = 0.5

switching frequencies are below 50 KHz in these applications. That is the reason for the around 50% of the ripple is acceptable for the inductor current.[42-48] For the simulation results, the MATLAB/SIMULINK has been used.

Figure 9 presents the voltages across the inductors. Since a positive voltage across an inductor charges the inductor current and the negative voltage discharges the current of the inductor, this figure easily can confirm that all of the inductors will begin to be charged and discharged simultaneously. The charging will be done in the ON-state time interval of the switch and the discharging process will happen at the OFF-state. Figure 10 illustrates the voltage across the different diodes in the proposed converter. From Figure 10A, as predicted in Section 1 for the states 1 and 2 for the ON and OFF-operational modes of the power switch, and as shown in Figure 1B,C, at the same time only one of the diodes D_1 and D_2 are activated. A negative voltage across a diode shows that the diode will be deactivated and a voltage with a positive amplitude equal to the diode's threshold voltage will activate the diode.

Also Figure 10B shows that the states of the diodes in the switched-capacitor side based on Figure 1B,C is truly estimated and when D_3, D_4, and D_6 are activated diode D_5 is deactivated and vice versa.

Figure 11A,B presents the voltages across the capacitors in the proposed power converter. An interesting result that easily can track by this figure is the voltage on the capacitor C_4 that is equal to the total of the voltages on the capacitors C_3 and C_5. This state had been predicted by the Equation (9).

Figure 12 shows the comparative curves to evaluate the efficiency of the proposed converter and the converters presented in Table 1 theoretically. According to this figure, efficiency is less for all of the converters for the low power applications. The reason is clear. Any converter losses a fixed amount of the power for the semiconductor components. So, when the power value is low, the efficiency is low too.[37-41] Other losses types for a power circuit are including the switching and dynamic losses. So, for the higher power values the efficiency is being more. As can be seen from this figure, the efficiency of the proposed converter is being more by increasing the output power and reaches the most efficient point at around 150 W. After this power, the proposed converter maintains its efficiency. For obtaining this curve, input and output voltages is fixed to 24 and 240 V, respectively and by changing the load value, different levels of the

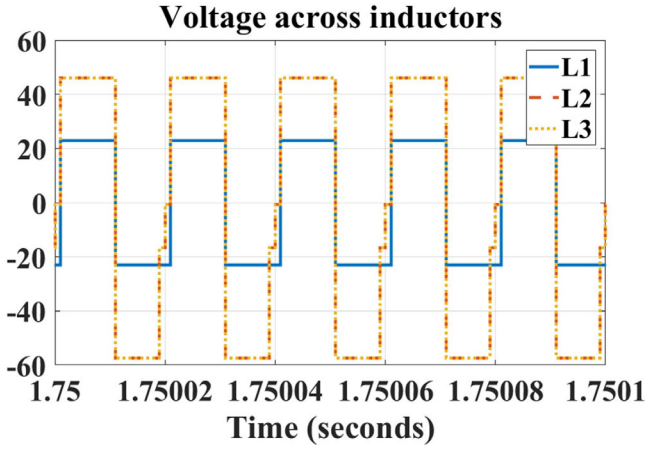


FIGURE 9 Voltage across inductors and charging and discharging time intervals

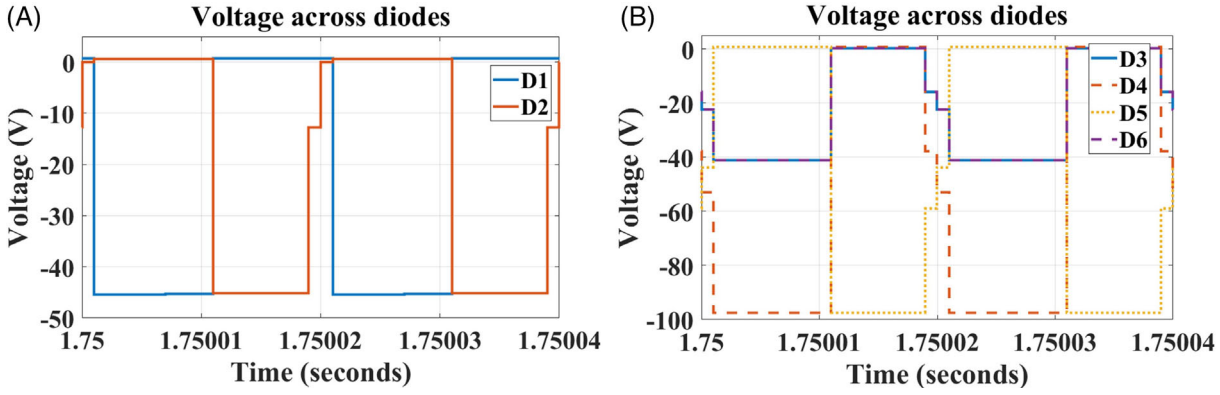


FIGURE 10 Voltage across, A, D_1, D_2, and B, D_3-D_6 for charging and discharging time intervals

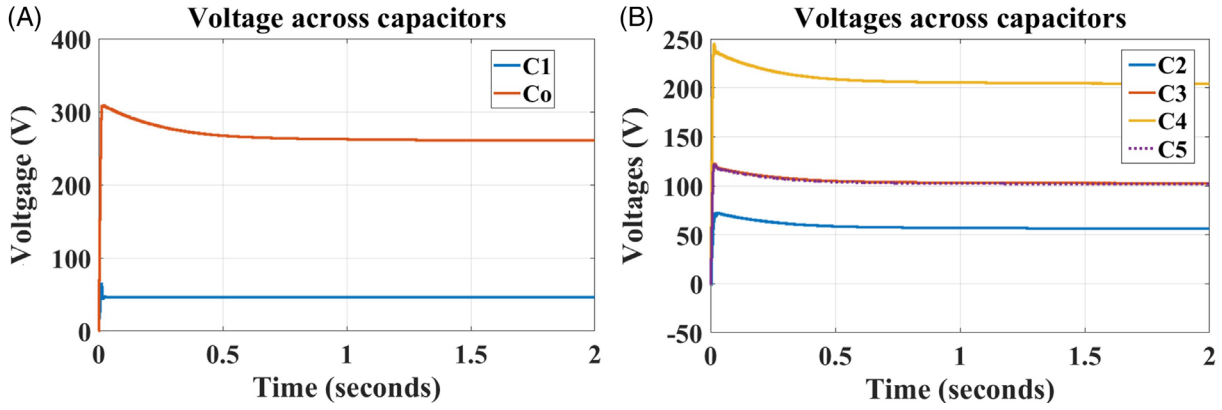
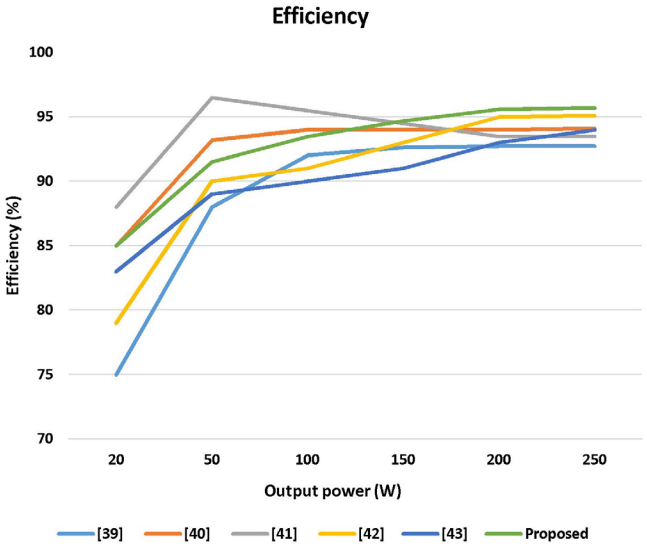


FIGURE 11 Voltage across, A, C_1, C_O, and B, C_2-C_5

FIGURE 12 Efficiency comparison for the proposed converter and other converter in Table 1



load currents are obtained. Since $P = V.I$, the different power values can be calculated for the output side. The average amount of the input current is reported through the oscilloscope in the MATLAB/SIMULINK environment and the input power is obtained through the same power equation. So, the efficiency easily can be found by $\eta = \frac{P_O}{P_{in}}$.

Figure 13A presents the implemented hardware. Since that this circuit has been designed to be used for the PV utilizations, the real value of these panels components and parameters are considered. For example, the input voltage and output power of the converter have been fixed at 24 V DC and 170 W that is the normal level of the voltage and the power for many of the PV panels like JIYANGYIN HAREON HR-200W/24. Differential probes are used to measure the voltage and currents of the components in the circuit. Test results are shown in Figure 13B-K. in some of these figure a coefficient is appearing on the figure that show the real measured value by the probes. For example, the (2.32 × 20) in Figure 13B illustrates that the volume on the differential probe has been adjusted on 20 and it shows the real measured value is 46.4 V. The driving signal at the gate-source and result voltage across drain-source pins are presented in Figure 13B. As can be seen in this figure, around 24 V is considered for the gate-source pins and for the 240 V DC at the output load, a voltage with around 46.6 V of amplitude drops at the drain-source pins. In comparison with the output voltage, this level of the mitigated voltage is considerable and approximately around 20% of the output voltage appears in switch. It is one of the main advantages of the proposed converter. This result shows that the output voltage is dividing on the other capacitors of the switched-capacitor cell. Figure 13C presents the input and output voltages. Since the duty cycle and the switching frequency are adjusted on 0.5 and 50 KHz, where 240 V DC is expected at the output ends, a voltage around 232 V DC is obtained that is a considerable result. The voltage across the inductors L_1 to L_3 are reported in Figure 13D,E. These figures can easily confirm that all of the inductors are charging and discharging simultaneously that is presented in Figures 1B,C, 2, 3, and 4. Charging and discharging mean that voltage on inductors

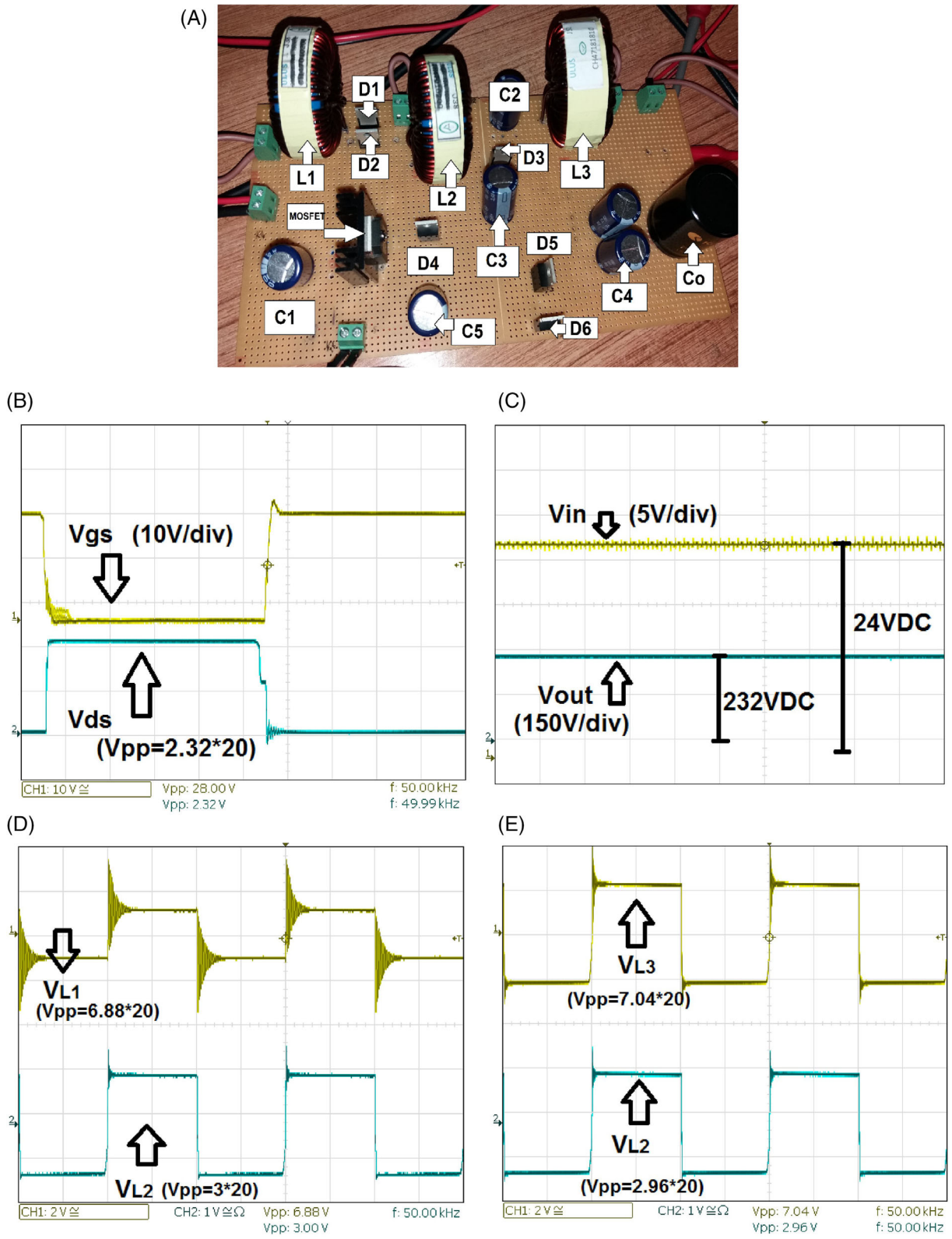


FIGURE 13 Experimental results. A, Implemented hardware, B voltage across the gate-source and drain-source pins of the power MOSFET, C, input–output voltages, voltages across, D, the inductors L_1 and L_2 and E, the inductors L_2 and L_3, and F, the diodes D_1-D_2, and G, D_3-D_4, and H, D_5-D_6, and on capacitors, I, C_1-C_2, J, C_3-C_4 and K, C_5-C_O

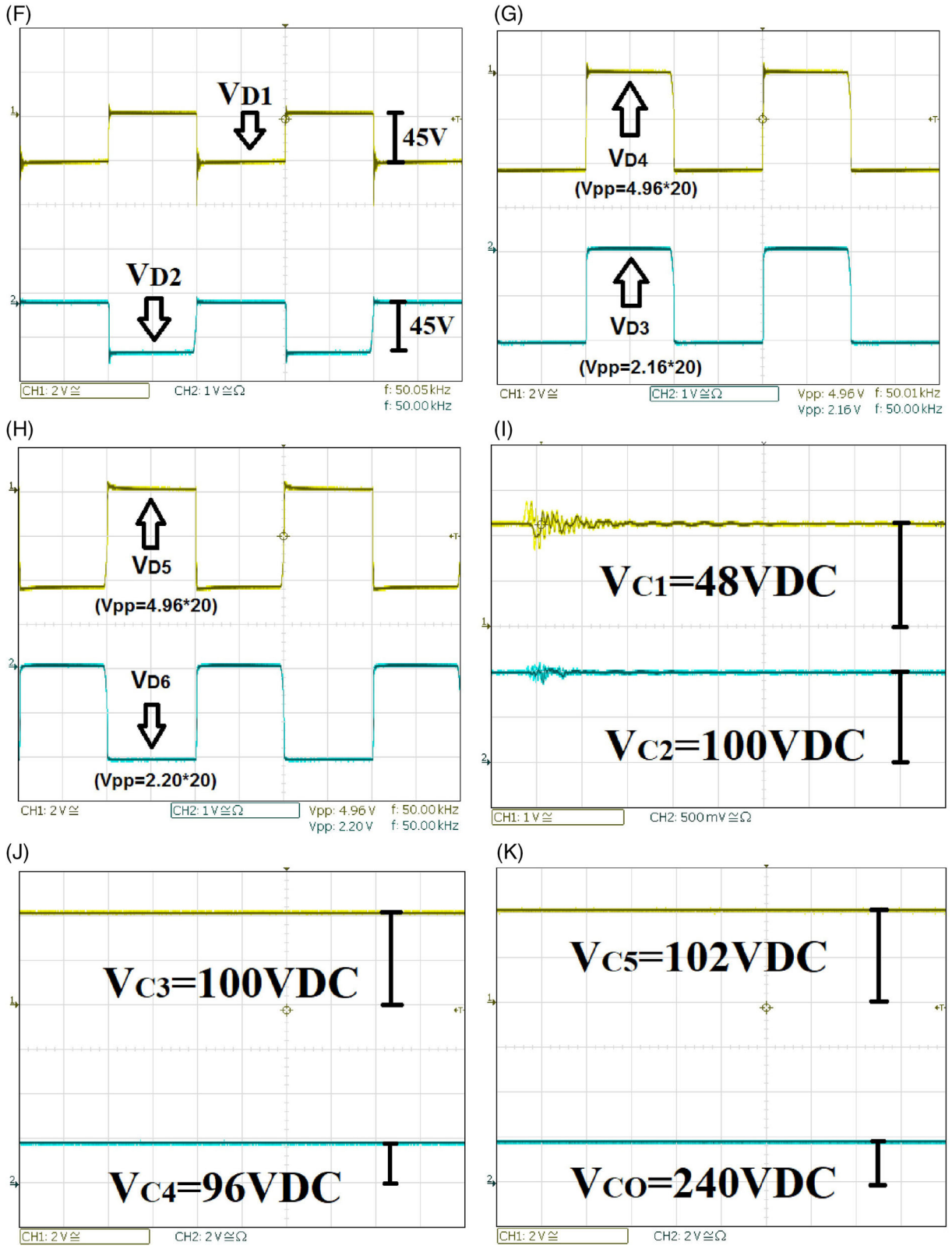


FIGURE 13 (Continued)

are positive and negative, so the current follows through the inductors are raising and falling respectively. But since the proposed converter has been designed to operate in the CCM, the average of the currents of the inductors always should be positive. Raising and falling of the current make the current ripples that is presented in Figures 4 and 8B.

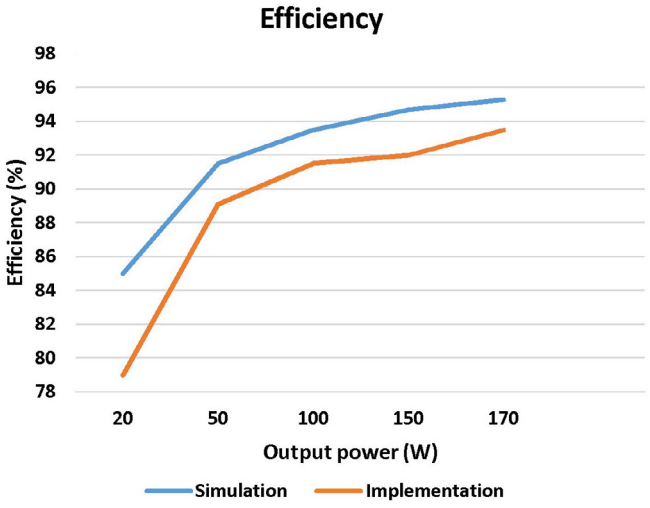


FIGURE 14 Efficiency assessment for the proposed converter by simulation and hardware test results

Figure 13F-H illustrates the voltages across the power diodes D_1 to D_6. Results confirm the theoretical investigations presented in Section 2 in the Figures 1B,C, 2, and 3 and the Equations (1) to (9). Diodes D_1 and D_2 and diodes D_5 and D_6 are activated asynchronously and the diodes D_3 and D_4 are activated simultaneously. Another important issue is the voltage stresses across the anode-cathode pins of the diodes. According to these results, the dropped voltage values reversely for the diodes D_1 to D_6 are 45, 45, 43.2, 99.2, 99.2, and 44 V, respectively. These levels of the voltages in comparison with the output voltage are completely less and tolerable. Figure 13I-K shows the voltages across capacitors C_1-C_2, C_3-C_4, and C_5-C_6, respectively. The voltages values are reported equal to 48, 100, 100, 96, 102, and 240 V DC, respectively for the capacitors C_1 to C_5 and C_O. The theoretical analysis shows that the 48, 96, 96, 96, 96, and 240 V DC are expected according to Equations (13) to (17) for these capacitors, respectively. There is a good matching between the measured results and the values are estimated through the mathematical analysis. The differences between some of these voltages can be considered as the losses on the internal resistances of the capacitors.

Figure 14 shows the efficiency curves for the proposed converter according to real test results and the simulation results presented in Figure 12. This figure shows that the efficiency in the real conditions of the laboratory-scaled prototype is closed to the results for the simulation. The difference between these two curves can be expressed as the internal resistance of the components and voltages droops across the power diodes and other slight parameters that have not been considered mathematically.

4 | CONCLUSION

A new switched-capacitor-based, transformer-less, and single-switched DC-DC power boost converter is presented in this study. Although the number of the power diodes, capacitors and inductors are more for the proposed topology in comparison with the classical boost and buck-boost converters, the voltage gain of the projected structure considerably is more and the converter suggests a mitigated-voltage stress on the power switch. These features will be more important when know for the duty cycle equal to 0.8, theoretically with 10 V DC as the input voltage, a voltage with 70 times greater than magnitude of the input voltage can be obtained at the output nodes and the dropped voltage on the drain-source pins will be equal to 175 V that is only the quarter of the output voltage. This feature can increase the reliability and long-life of the converter and decrease the power losses on the switch. The reaction of the circuit under CCM operational condition was analyzed and the voltage and currents of the components were investigated mathematically and practically by a 170 W implemented hardware.

ACKNOWLEDGEMENTS

This work was supported by the National Natural Science Foundation of China under Grant Nos. 61702238, 61862027, 61762043, and 61661022, and the Science and Technology Foundation of Educational Commission of Jiangxi Province of China under Grant Nos. GJJ170316 and GJJ180264.

PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/2050-7038.12569.

ORCID

Davood Ghaderi https://orcid.org/0000-0003-2234-3453

REFERENCES

1. Liu J, Wu J, Qiu J, Zeng J. Switched Z-source/quasi-Z-source DC-DC converters with reduced passive components for photovoltaic systems. *IEEE Access*. 2019;7:40893-40903. https://doi.org/10.1109/ACCESS.2019.2907300.
2. Hang L, Subramaniam U, Bayrak G, Moayedi H, Ghaderi D, Minaz MR. Influence of a proposed switching method on reliability and total harmonic distortion of the quasi Z – source inverters. *IEEE Access*. 2020;8:33088–33100. https://doi.org/10.1109/ACCESS.2020.2973797.
3. Gu Y, Chen Y, Zhang B, Qiu D, Xie F. High step-up DC-DC converter with active switched LC-network for photovoltaic systems. *IEEE Trans Energ Conver*. 2019;34(1):321-329. https://doi.org/10.1109/TEC.2018.2876725.
4. Bellinaso LV, Figueira HH, Basquera MF, Vieira RP, Gründling HA, Michels L. Cascade control with adaptive voltage controller applied to photovoltaic boost converters. *IEEE Trans Ind Appl*. 2019;55(2):1903-1912. https://doi.org/10.1109/TIA.2018.2884904.
5. Zhao X, Chen C, Lai J. A high-efficiency active-boost-rectifier-based converter with a novel double-pulse duty cycle modulation for PV to DC microgrid applications. *IEEE Trans Pow Electron*. 2019;34(8):7462-7473. https://doi.org/10.1109/TPEL.2018.2878225.
6. Urtasun A, Samanes J, Barrios EL, Sanchis P, Marroyo L. Control of a photovoltaic array interfacing current-mode-controlled boost converter based on virtual impedance emulation. *IEEE Trans Ind Electron*. 2019;66(5):3496-3506. https://doi.org/10.1109/TIE.2018.2856192.
7. Das D, Madichetty S, Singh B, Mishra S. Luenberger observer based current estimated boost converter for PV maximum power extraction—a current sensorless approach. *IEEE J Photovolt*. 2019;9(1):278-286. https://doi.org/10.1109/JPHOTOV.2018.2877418.
8. Jia K, Chen J, Xuan Z, Wang C, Bi T. Active protection for photovoltaic DC-boosting integration system during FRT. *IET Gener Transm Dis*. 2019;13(18):4081-4088. https://doi.org/10.1049/iet-gtd.2019.0540.
9. Ghader'I D, Kiran Maroti P, Sanjeevikumar P, Bo HolmNielsen J, Hossain E, Nayyar A. A modified step up converter with small signal analysis based controller for renewable resource applications. *Appl Sci*. 2020;10(1):1-23.
10. Liu L, Li D, Yao L. Non-isolated high step-up DC-DC conversion circuits forphotovoltaic system. *Int Trans Electr Energ Syst*. 2020;30:e12192. https://doi.org/10.1002/2050-7038.1219218.
11. Banerjee S, Rana N, Khuntia MR. Closed-loop control and performance analysis of a high-gain buck-boost converter with optimized type III controller. *Int Trans Electr Energ Syst*. 2020;30:e12158. https://doi.org/10.1002/2050-7038.12158.
12. Priyadarshi A, Kar PK, Karanki SB. A wide load range ZVS high voltage gain hybrid DC-DC boost converter based on diode-capacitor voltage multiplier circuit. *Int Trans Electr Energ Syst*. 2020;30:e12171. https://doi.org/10.1002/2050-7038.12171.
13. Wu B, Li S, Ma Smedley K. A new single-switch isolated high-gain hybrid boosting converter. *IEEE Trans Ind Electron*. 2016;63(8):4978-4988. https://doi.org/10.1109/TIE.2016.2554542.
14. Du H, Huo Z. PSM control technique for primary-side regulating fly-back converters. *IET Pow Electron*. 2018;11(3):531-538. https://doi.org/10.1049/iet-pel.2017.0332.
15. Karimian F, Nahavandi A. Design and analysis of a new structure of non-isolated DC-DC cuk-boost converter with high voltage gain. *IET Pow Electron*. 2019;12(3):530-540. https://doi.org/10.1049/iet-pel.2018.5497.
16. Pires VF, Cordeiro A, Foito D, Silva JF. High step-up DC-DC converter for fuel cell vehicles based on merged quadratic boost–Ćuk. *IEEE Trans Veh Technol*. 2019;68(8):7521-7530. https://doi.org/10.1109/TVT.2019.2921851.
17. Huang R, Hong F, Ghaderi D. Sliding mode controller based E bike charging station for photovoltaic applications. *Int Trans Electr Energ Syst*. 2019;30(4):1–25. https://onlinelibrary.wiley.com/doi/abs/10.1002/2050-7038.12300.
18. Jiang W, Chincholkar SH, Chan C. Investigation of a voltage-mode controller for a DC-DC multilevel boost converter. *IEEE Trans Circuits Syst II Exp Briefs*. 2018;65(7):908-912. https://doi.org/10.1109/TCSII.2017.2723660.
19. Veerachary M, Shaw P. Controller design and analysis for fifth-order boost converter. *IEEE Trans Ind Appl*. 2018;54(5):4894-4907. https://doi.org/10.1109/TIA.2018.2843758.
20. Hariharan K, Kapat S. Near optimal controller tuning in a current-mode DPWM boost converter in CCM and application to a dimmable LED array driving. *IEEE J Emerg Sel Topics Pow Electron*. 2019;7(2):1031-1043. https://doi.org/10.1109/JESTPE.2018.2817840.
21. de Carvalho Neto JT, de Oliveira Cavalcanti AL, Ortiz Salazar A. Design and implementation of DSP-based H-infinity robust controller for a boost converter. *IEEE Lat Am Trans*. 2018;16(11):2766-2774. https://doi.org/10.1109/TLA.2018.8795118.
22. Seo S, Choi HH. Digital implementation of fractional order PID-type controller for boost DC-DC converter. *IEEE Access*. 2019;7:142652-142662. https://doi.org/10.1109/ACCESS.2019.2945065.
23. Wu H, Mu T, Ge H, Xing Y. Full-range soft-switching-isolated buck-boost converters with integrated interleaved boost converter and phase-shifted control. *IEEE Trans Pow Electron*. 2016;31(2):987-999. https://doi.org/10.1109/TPEL.2015.2425956.
24. Mangu B, Akshatha S, Suryanarayana D, Fernandes BG. Grid-connected PV-wind-battery-based multi-input transformer-coupled bidirectional DC-DC converter for household applications. *IEEE J Emerg Sel Topics Pow Electron*. 2016;4(3):1086-1095. https://doi.org/10.1109/JESTPE.2016.2544789.

25. Ahmed HF, Cha H, Khan AA, Kim H. A family of high-frequency isolated single-phase Z-source AC-AC converters with safe-commutation strategy. *IEEE Trans Pow Electron*. 2016;31(11):7522-7533. https://doi.org/10.1109/TPEL.2016.2539216.
26. Li S, Zheng Y, Wu B, Smedley KM. A family of resonant two-switch boosting switched-capacitor converter with ZVS operation and a wide line regulation range. *IEEE Trans Pow Electron*. 2018;33(1):448-459. https://doi.org/10.1109/TPEL.2017.2669841.
27. Nguyen M, Duong T, Lim Y. Switched-capacitor-based dual-switch high-boost DC-DC converter. *IEEE Trans Pow Electron*. 2018;33(5):4181-4189. https://doi.org/10.1109/TPEL.2017.2719040.
28. Stala R, Waradzyn Z, Penczek A, Mondzik A, Skała A. A switched-capacitor DC-DC converter with variable number of voltage gains and fault-tolerant operation. *IEEE Trans Ind Electron*. 2019;66(5):3435-3445. https://doi.org/10.1109/TIE.2018.2851962.
29. Lee S, Do H. High step-up coupled-inductor cascade boost DC-DC converter with lossless passive snubber. *IEEE Trans Ind Electron*. 2018;65(10):7753-7761. https://doi.org/10.1109/TIE.2018.2803731.
30. Barry BC, Hayes JG, Rylko MS, et al. Small-signal model of the two-phase interleaved coupled-inductor boost converter. *IEEE Trans Power Electron*. 2018;33(9):8052-8064. https://doi.org/10.1109/TPEL.2017.2765920.
31. G. Spiazzi, "Analysis and design of the soft-switched clamped-resonant interleaved boost converter," in *CPSS Trans Pow Electron Appl*, vol. 4, no. 4, pp. 276–287, 2019.doi: https://doi.org/10.24295/CPSSTPEA.2019.00026, 4
32. Rana N, Kumar M, Ghosh A, Banerjee S. A novel interleaved tri-state boost converter with lower ripple and improved dynamic response. *IEEE Trans Ind Electron*. 2018;65(7):5456-5465. https://doi.org/10.1109/TIE.2017.2774775.
33. Chen H, Lu C, Rout US. Decoupled master-slave current balancing control for three-phase interleaved boost converters. *IEEE Trans Pow Electron*. 2018;33(5):3683-3687. https://doi.org/10.1109/TPEL.2017.2760887.
34. Yi J, Choi W, Cho B. Zero-voltage-transition interleaved boost converter with an auxiliary coupled inductor. *IEEE Trans Pow Electron*. 2017;32(8):5917-5930. https://doi.org/10.1109/TPEL.2016.2614843.
35. Ghaderi D, Bayrak G. Performance assessment of a high powered boost converter for photovoltaic residential implementations. *Elektron Elektrotech*. 2019;25(6):40-47. https://doi.org/10.5755/j01.eie.25.6.24825.
36. Hart DW. *Power Electronics*. 2 Pennsylvania Plaza New York City: McGraw-Hill; 2011 ISBN: 007741795X.
37. Gules R, Pfitscher LL, Franco LC. An interleaved boost DC-DC converter with large conversion ratio. *Proc IEEE Int Symp Ind Electron*. 2003;1:411-416. https://ieeexplore.ieee.org/document/1267284.
38. Wu G, Ruan X, Ye Z. Nonisolated high step-up DC-DC converters adopting switched-capacitor cell. *IEEE Trans Ind Electron*. 2015;62(1):383-393. https://doi.org/10.1109/TIE.2014.2327000.
39. Tang Y, Wang T, He Y. A switched-capacitor-based active-network converter with high voltage gain. *IEEE Trans Pow Electron*. 2014;29(6):2959-2968. https://doi.org/10.1109/TPEL.2013.2272639.
40. Galigekere P, Kazimierczuk MK. Analysis of PWM Z-source DC-DC converter in CCM for steady state. *IEEE Trans Circuits Syst I, Reg Papers*. 2012;59(4):854-863.
41. Shen H, Zhang B, Qiu D, Zhou L. A common grounded Z-source DC-DC converter with high voltage gain. *IEEE Trans Ind Electron*. 2016;63(5):2925-2935. https://doi.org/10.1109/TIE.2016.2516505.
42. Ma L, Kerekes T, Rodriguez P, Jin X, Teodorescu R, Liserre M. A new PWM strategy for grid-connected half-bridge active NPC converters with losses distribution balancing mechanism. *IEEE Trans Pow Electron*. 2015;30(9):5331-5340. https://doi.org/10.1109/TPEL.2014.2387152.
43. Zhou L, Gao F, Xu T. A family of neutral-point-clamped circuits of single-phase PV inverters: generalized principle and implementation. *IEEE Trans Pow Electron*. 2017;32(6):4307-4319. https://doi.org/10.1109/TPEL.2016.2587660.
44. Wang L, Shi Y, Shi Y, Xie R, Li H. Ground leakage current analysis and suppression in a 60-kW 5-level T-type transformerless SiC PV inverter. *IEEE Trans Pow Electron*. 2018;33(2):1271-1283. https://doi.org/10.1109/TPEL.2017.2679488.
45. Khan AA, Cha H. Dual-buck-structured high-reliability and high-efficiency single-stage buck–boost inverters. *IEEE Trans Ind Electron*. 2018;65(4):3176-3187. https://doi.org/10.1109/TIE.2017.2752145.
46. Zaid SA, Kassem AM. Review, analysis and improving the utilization factor of a PV-grid connected system via HERIC transformerless approach. *Renew Sustain Energy Rev*. 2017;73:1061-1069. https://doi.org/10.1016/j.rser.2017.02.025.
47. Saridakis S, Koutroulis E, Blaabjerg F. Optimization of SiC-based H5 and conergy-NPC transformerless PV inverters. *IEEE J Emerg Sel Topics Pow Electron*. 2015;3(2):555-567. https://doi.org/10.1109/JESTPE.2014.2332253.
48. Zhang L, Sun K, Xing Y, Xing M. H6 transformerless full-bridge PV grid-tied inverters. *IEEE Trans Pow Electron*. 2014;29(3):1229-1238. https://doi.org/10.1109/TPEL.2013.2260178.

How to cite this article: Hu D, Yin A, Ghaderi D. A transformer-less single-switch boost converter with high-voltage gain and mitigated-voltage stress applicable for photovoltaic utilizations. *Int Trans Electr Energ Syst*. 2020;30:e12569. https://doi.org/10.1002/2050-7038.12569