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RESEARCH ARTICLE

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Genetic algorithm based reference current control extraction based shunt active power filter

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Abstract

Traditional approaches towards proportional-integral (PI) controller tuning often fail to provide optimum gain values in situations where shunt active power filter (SAPF) is connected to systems containing complex, dynamic, and nonlinear loads. Optimum gain values are, however, crucial in the generation of compensating currents with less transient and steady-state error, that would nullify the harmonic currents in a short time. This work proposes two soft computing techniques, genetic algorithm (GA) and Queen Bee assisted GA (QBGA) for better controller tuning to obtain optimum gain values to switch SAPF. These algorithms are used in local search technique mode to arrive at the optimal solutions based on the desired characteristics. The PI controller controls the voltage of the DC capacitor to generate the required compensating current. The proposed algorithms are practical since reliable solutions are obtained with a limited number of iterations. Implementation of the suggested algorithm reduces the THD of supply current to less than 5%, in compliance with IEEE-519 standards. The system performance is evaluated through MATLAB simulation tool. Suitable hardware model is also developed and tested for validating the simulation results. The hardware results are found in close agreement with simulation results. The highlight of this work is the introduction of QBGA algorithm as a novel technique for tuning of PI controller for SAPF.

KEYWORDS

genetic algorithm, pulse width modulation, queen beegenetic algorithm, shunt active power filter, total harmonic distortion

List of Symbols and Abbreviations: ADC, Analog-to-Digital Converters; DRC, Dual-Repetitive Controller; GA, genetic algorithm; ICC, Independent Current Control; IGBTs, Insulated-Gate Bipolar Transistors; LUnC, Load Unbalance Compensation; MRAFC, Model Reference Adaptive Fuzzy Control; PCC, Point of Common Coupling; PI, proportional-integral; PSO, Particle Swarm Optimization; RECKF, Robust Extended Complex Kalman Filter; SAPF, shunt active power filter; QBGA, Queen Bee assisted GA.

1 | INTRODUCTION

The ever-increasinguse of equipment's like static power converters, electronic chokes etc. harms the quality of power supply. Though initially the supply voltage and current are sinusoidal, eventually the supply current tends to non-sinusoidal with significant harmonic content whenever nonlinear loads are applied to the system. The harmonic components in the load current do not contribute to active power, and therefore they have to be eliminated if the power quality is to be improved.[1,2] Also, in three-phase unbalanced systems, harmonic currents flow in the neutral conductors causing low efficiency and reduced power factor.[3] Traditionally, passive filters are used to mitigate harmonics and supply reactive power to the loads.[4] But, passive filters suffer from the following; bulkiness, ageing, possibility to resonate with supply impedance if tuning is improper. Recently, better alternative active filters are developed to mitigate the current/voltage harmonics in the supply side.[5,6] The advantages of an active filter are its use of passive components of smaller rating, and basically, it is a regulated system, capable of dealing with randomly fluctuating harmonic currents.[7] To compensate the voltage harmonics active filter is connected in series at the point of common coupling (PCC) and to compensate current harmonics active filter is connected in parallel at PCC. In paper,[8] the performance of SAPF with different control schemes such as instantaneous p-q theory, modified p-q theory and i_d - i_q schemes are presented. It also deals with particle swarm optimization (PSO) algorithm for optimizing PI controller gains. In,[9] three control schemes viz, neural network, fuzzy logic and genetic algorithm are described and simulated using MATLAB tool for switching SAPF. In the past, significant research has been carried out in the field of genetic algorithms which are simple, approximation techniques and suitable stochastic optimization methods.

In,[10] an adaptive fuzzy-sliding control system is derived, and the asymptotic stability of the closed-loop system is tested in the sense of Lyapunov. In this sliding-mode control method, the control effort is approximate as the unknown equivalent control term and sliding term. This method is tested by simulation, and corresponding THD value is reduced from 24.71% to 1.59%. In,[11] the SAPF is constructed with three single-phase full-bridge converters sharing the same dc-bus voltage. Two control strategies under modified synchronous reference frame (SRF) schemes, namely independent current control (ICC) and load unbalance compensation (LUnC), are discussed. The state feedback control technique is employed to calculate the gain values of the PI controller. The THD of the supply current gets reduced from 20% to 5%. In,[12] a new controller, which a variant of Kalman Filter, called the robust extended complex kalman filter (RECKF) is presented. The controller outperforms all the variants of the Kalman filter for the SAPF system and is proven experimentally. The RECKF has performed better when compared tothe PI controller for the given system. Step response and phase response arevalidated, but no direct stability analysis is carried out in this work. In this control technique, the THD reduces from 24.9% to 4.46%. In,[13] a model reference adaptive fuzzy control (MRAFC) is presentedfor the single-phase SAPF to cater to static and dynamic performance specifications. The system is modelled and validated through simulation results. The supply current THD is reduced to 3.98%. In,[14] a neural network-based PI control and dual-repetitive controller (DRC) is used for the SAPF. A repetitive controller is used to ensure current tracking accuracy in DRC, and another controller is used to enhance dynamic system response. To improve response speed byPI parameters are tuned by the neural networks. The experimental results of the proposed model in[14] show that the THD is reduced to 4.68%.

This work provides the design, simulation, and experimental study of a SAPF to mitigate the supply current harmonics and provide required reactive power to the nonlinear load. The three-phase three-level diode clamped multilevel inverter, and DC capacitor combination serves as the SAPF. The control algorithms proposed are based on genetic algorithm (GA), and Queen-Bee assisted Genetic Algorithm (QBGA) for generating reference currents for the SAPF. The performances of GA assisted controllers are validated under transientas well assteady-state conditions. The switching signals are generated using the sampled reference phase voltage magnitudes, and centers the switching times for the middle vectors, as in the case of conventional space vector PWM.[15,16] The performance of the system using GA and QBGA is simulated in MATLAB platform. The simulation results are validated using an experimental prototype model. The results of the simulation and experimentinferred that the SAPF systems maintain the THD of the supply current within limits.

The main contribution of the paper is to synthesize the gains of a PI controller for SAPF system using GA and QBGA, and implement the same on a digital platform and validate the performance experimentally. For synthesizing the parameters of the controller, GA and QBGA have been employed since the system involves nonlinearity. To the best of the knowledge, in literature, QBGA based method has not been employed for synthesizing the parameters of the controller for a SAPF system. In addition, after carrying out extensive simulation studies, QBGA algorithm was finalized since it offers more flexibility than the existing techniques and yields optimal system performance. Furthermore, the bio-inspired process enabled us to reach the global minimum in a smaller number of iteration (epochs). The QBGA technique also helped in extracting realizable values for the controller parameters so that hardware implementation

(on a digital platform) was carried out with consummate ease. Since hardware realization was also a major objective of the research work, QBGA was chosen over the existing tuning algorithms. The organization of the paper is as follows:

The design of the SAPF is dealt with in section 2; the methodology of GA and QBGA are presented in section 3 and 4, respectively. Hardware and simulation results are described in section 5. Conclusion and scope for future workare offered in section 6.

2 | SHUNT ACTIVE POWER FILTER

2.1 | Compensation principle

The control objective of SAPF is to draw/supply a compensating current I_c from/to the utility grid, such that it cancels the harmonics current on the AC side.[7] The other use of SAPFcould be to compensate for the reactive power at the source side. The instantaneous current and voltage of the source are expressed as follows:

$$i_s(t) = i_L(t) - i_C(t) \tag{1}$$

$$v_s(t) = V_m \sin\omega t \tag{2}$$

where $i_s(t)$, $i_L(t)$, i_C (t) are instantaneous values of source, load, and filter current, respectively: $v_s(t)$, and $V_m$areinstantaneous and peak value of source voltage. Nonlinear load injects the nonlinear components in the load current and Fourier series expression of the load current is represented as follows:

$$i_L(t) = I_1 \sin(\omega t + \emptyset_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \emptyset_n) \tag{3}$$

The instantaneous power of the load is given as

$$p_L(t) = v_s(t) i_L(t) \tag{4}$$

$$p_L(t) = V_m \sin\omega t \left\{ I_1 \sin(\omega t + \emptyset_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \emptyset_n) \right\} \tag{5}$$

The Equation (5) is expressed as follows:

$$p_L(t) = V_m \mathrm{I}_1 \sin^2\omega t \cos\emptyset_1 + V_m \mathrm{I}_1 \sin\omega t \cos\omega t \sin\emptyset_1 + V_m \sin\omega t \sum_{n=2}^{\infty} I_n \sin(n\omega t + \emptyset_n) \tag{6}$$

Now, $p_L(t)$ can be resolved as

$$p_L(t) = p_f(t) + p_r(t) + p_h(t), \tag{7}$$

where $p_f(t)$ is real (fundamental) power, $p_r(t)$is the reactive power and $p_h(t)$is the harmonic-power. From (7), the fundamental (real) power drawn by the load is

$$p_f(t) = V_m I_1 sin^2\omega t \cos\emptyset_1 = v_s(t) i_s(t) \tag{8}$$

$$\text{with } i_s(t) = I_1 \sin\omega t \cos\emptyset_1 = I_{sm} \sin\omega t = I_{max} \sin\omega t \tag{9}$$

$$\text{where } I_{max} = I_1 \cos\emptyset_1 \tag{10}$$

In case, the total reactive and harmonic power are compensated by the active power filter then the source current $i_s(t)$ will be in phase with the source voltage and would be sinusoidal as well. The compensated three-phase source currents are

$$i^*_{ca}(t) = P_f(t)/V_s(t) = I_1 \cos\emptyset_1 sin\omega t = \mathrm{I}_{max} sin\omega t \tag{11}$$

Similarly, we have

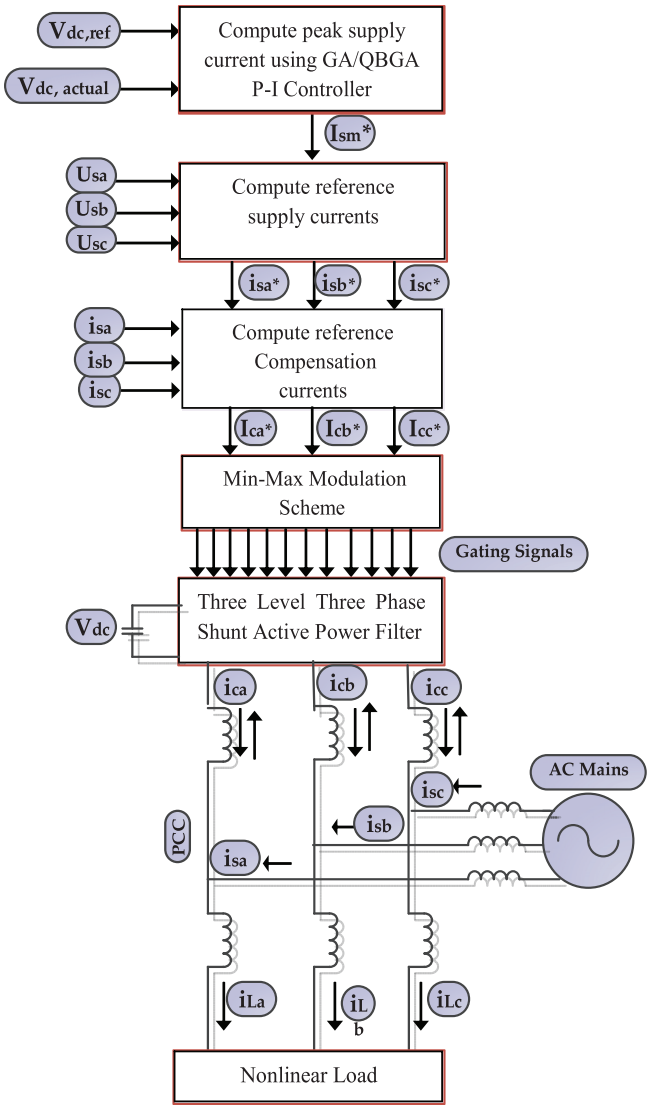


FIGURE 1 Control scheme for SAPF

$$i_{cb}^{*}(t) = I_{max}(\sin\omega t - 120) \tag{12}$$

$$i_{cc}^{*}(t) = I_{max}(\sin\omega t + 120) \tag{13}$$

The control scheme of the SAPF system is presented in Figure 1. In this work, two control algorithms, that is GA and QBGA are implemented to find the optimum gain values for the PI controller and to estimate the maximum value of supply current i_{sm}^{*}. The instantaneous reference supply currents $\left(i_{sa}^{*}, i_{sb}^{*} \text{ and } i_{sc}^{*}\right)$ are computed using I_{sm} and unit current vectors(U_{sa}, U_{sb} *and* U_{sc}). The instantaneous compensation currents $\left(i_{ca}^{*}, i_{cb}^{*} \text{ and } i_{cc}^{*}\right)$ are derived using the reference currents $\left(i_{sa}^{*}, i_{sb}^{*} \text{ and } i_{sc}^{*}\right)$ and by sensing the actual supply currents(i_{sa}, i_{sb} *and* i_{sc}). Min-max controller is used to measuring the minimum and maximum value of the compensation current.

2.2 | Space vector PWM technique

In the proposed scheme, the independent individual pole voltages are generated by comparing the reference phase voltage with the triangular carrier signal.[17] A common-mode voltage, V_{offset}, is added to the reference phase voltages to get the maximum possible peak of the fundamental phase voltage, the magnitude ofV_{offset}, is given by

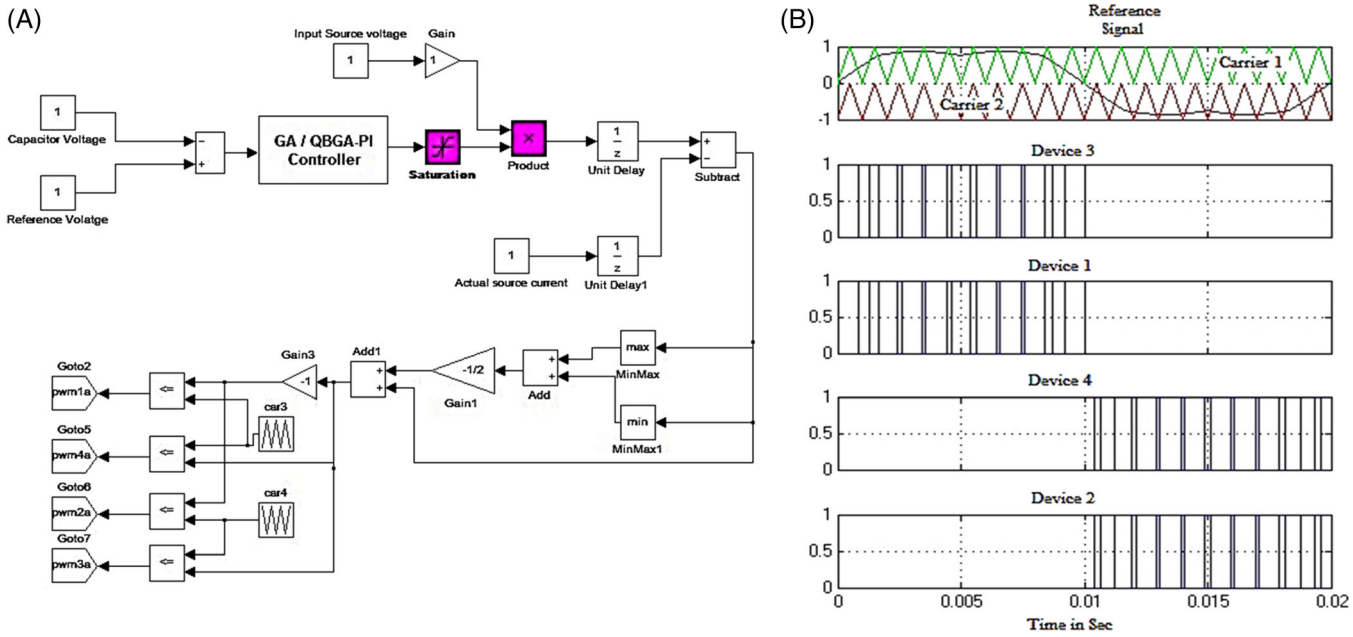


FIGURE 2 A, Generation of R-phase PWM pulses. B, Simulation output: PWM pulses for R-phase

$$V_{offset} = -\frac{(V_{min} + V_{max})}{2} \tag{14}$$

Where V_{min} and $V_{max}$are the minimum and maximum magnitudes of the three sampled reference phase voltages in a sampling interval. In every sampling interval, the active inverter switching vectors being centred due to the addition of V_{offset}, and which leads the SPWM technique equivalent to the space vector PWM technique presented in.[18-20] For generate PWM for the multilevel inverters, the SPWM technique compares the reference phase voltage signals with a number of symmetrical level-shifted carrier waves. To achieve this algorithm in the n-level inverter, (n-1) level-shifted carrier waves are required for comparison with the sinusoidal references. The maximum value of the input supply current is measured from the output of the PI controller. The per-unit value of the source voltage is multiplied by the output of the PI controller; the resultant value provides the reference current to the filter circuit. The filter compensation current through unit delay gain is generated by subtracting the measured source current from the reference current. Min-max controller is used to measuring the minimum and maximum value of the compensationcurrent, and it is added with negative gain amplifier. The waveform of R-phase reference voltage and triangular carriers for a PWM generation are shown in Figure 2A and B.

3 | GENETIC ALGORITHM

The principles used by in Genetic Algorithms (GAs) in searching are based on natural selection and genetics. In GAs, the decision variables of search problems are encoded into strings of alphabets with finite length. These strings are referred to as chromosomes, and they are the candidate solution to the search problem. The alphabets of the stringsare referred to as genes. Genetic Algorithm is used for optimization problems where the functions to be minimized non-convex and is not known.[21,22] For implement, the natural selection for obtaining the right solutions, a metric for distinguishing solutions are required. The measure is a mathematical function called fitness function is given in Equation (15).

$$\mathrm{ISE} = \int_0^T \left(V_{ref} - V_{dc}\right)^2 \tag{15}$$

Where ISE = integral square error between actual capacitor voltage and reference dc voltage.

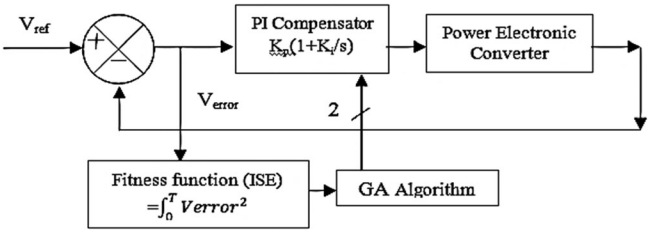


FIGURE 3 Block diagram of PI tuning using GA[23,24]

3.1 | Methodology

A population of candidate solutions in GAs are called individuals creatures or phenotypes; an optimization problem is evolved towards better solutions. A set of properties are associated with each candidate solution which can be mutated and altered traditionally. Solutions are represented in binary as strings of 0 second and 1 second, but other encodings are also possible like an entirely integer-based genetic algorithm. The block diagram of PI tuning using GA is shown in Figure 3. During the tuning phase, an ideal characteristic of power electronic converter is used. Steps to achieve optimization using genetic algorithm is explained in the flow chart is shown in Figure 4. The general step involved in optimization using GA is illustrated in Table 1.

4 | QUEEN BEE GENETIC ALGORITHM

Queen Bee assisted GA is an improvement over traditional GA, which is again biologically inspired by Bees in a Beehive. A prime force of a bee-hive is the queen bee, and its survival is essential for the endurance of the hive.[24,25] The selection and the crossover with the best solution, to make it similar to the swarm-based techniques in terms of the cognition. This technique results in better performance in terms of iterations and accuracy in comparison with traditional Genetic Algorithm. To achieve optimization using genetic algorithm is explained in the flow chart, as shown in Figure 5. The steps involved to perform optimization using Queen Bee assisted Genetic Algorithm.

Step 1: *Generation of bees*: The foremost step is the generation of bees within the constrained solution space. B_1, B_2... B_i...B_n represents the bees, where n stands for bee's population size.

Step 2: *Identification of queen Bee* B_q: The bees are evaluated based on the cost function and the one contributing to least cost function is selected as queen bee, where F_i is the fitness function. $B_q = Max\frac{1}{1+F_i}$

Step 3: *Mating Flight or Reproduction*: The re-production of next-generation bees is done by the mating fight of the queen bee. All drones may not fly fast to reach a queen, which gives a place for incorporating a probability of recombination associated with each drone. Recombination probability, p_r, is fixed at a suitable value between zero and One. The probability associated with each drone is denoted as p_i.

Step 3 (cont.): The drone combines with the queen to produce two virgin bees for *p*i *p*r. The recombination of the drone with the queen bee is precisely devised the same as a crossover in standard GA. Recombination produces two offspring, and among the two, only the fittest alone survives, and the other one is discarded and is equivalent to killing by the virgin queen bee.

Step 4: No recombination takes for pi <pr, and hence, there is no offspring. After steps (3) and (4), that is at the end of reproduction, the population of virgin queen bees is mostly less than n.

Step 5: Terminate the program if termination criterion is reached; else go to step (6). The new queen bees are selected as the optimum solution when termination occurs. The termination criterion is taken as 50 iterations.

Step 6: *Formation of the new population for next mating flight*: All drones after mating with the queen bee die, and hence, drones of population size (n − 1) are now randomly generated once again for the next reproduction. The randomly generated drones and new queen bee form the population for the next generation and go to step (3).

5 | HARDWARE AND SIMULATION

5.1 | Hardware setup

To validate the actual performance of the proposed GA, and QBGA method, an experimental model has been implemented for the 140 V, 50 Hz supply system. The hardware specifications are presented in Table 2. The detailed

FIGURE 4 Flowchart of the GA tuning algorithm

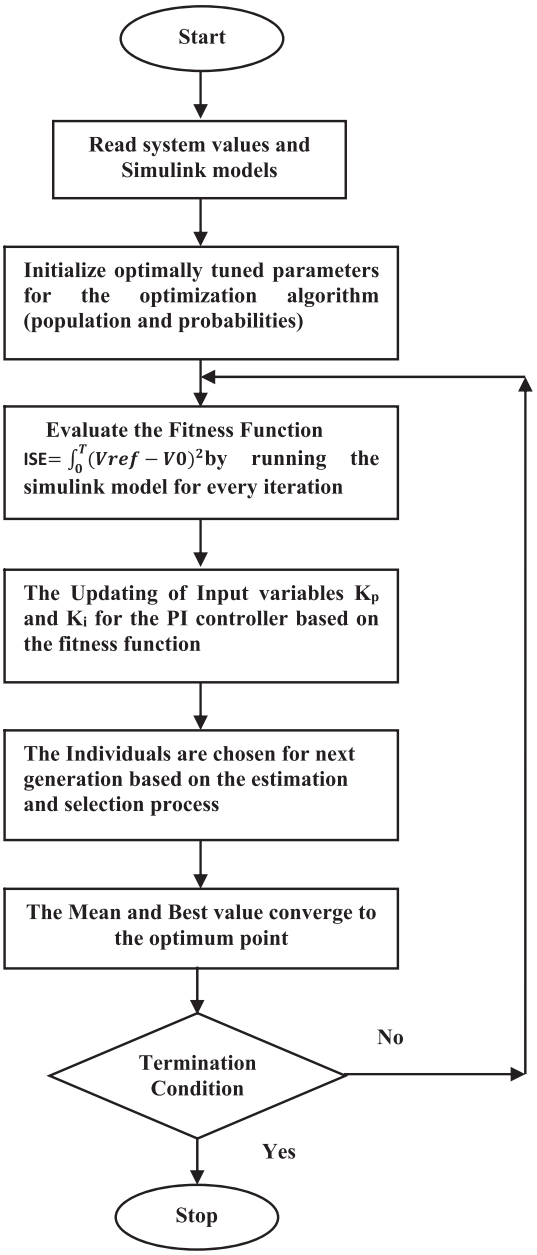


TABLE 1 General steps involved in optimization

Creation	uniform, feasible
Fitness scaling	Rank-based, proportional, top (truncation), shift linearly
Selection	Roulette, stochastic uniform selection (SUS), tournament, uniform, the remainder
Crossover	Arithmetic, heuristic, intermediate, scattered, single point, two points
Mutation	Adaptive feasible, Gaussian, Uniform.
Plotting	Best fitness, best individual, the distance among individuals, diversity of the population, exception of individuals, max constraint, range, selection index, stopping conditions.

hardware block diagram and hardware setup are given in Figure 6A,B, respectively. The compensation current is generated for the filter circuit by comparing the actual and reference dc capacitor voltage and then it is multiplied with input unit vector voltage. The control system consists of voltage and current acquisition circuitry. Hall Effect current transducers (LTS 25-NP) are used to measure the load currents, and potential transducers (LV 25-P) are used to sense the load

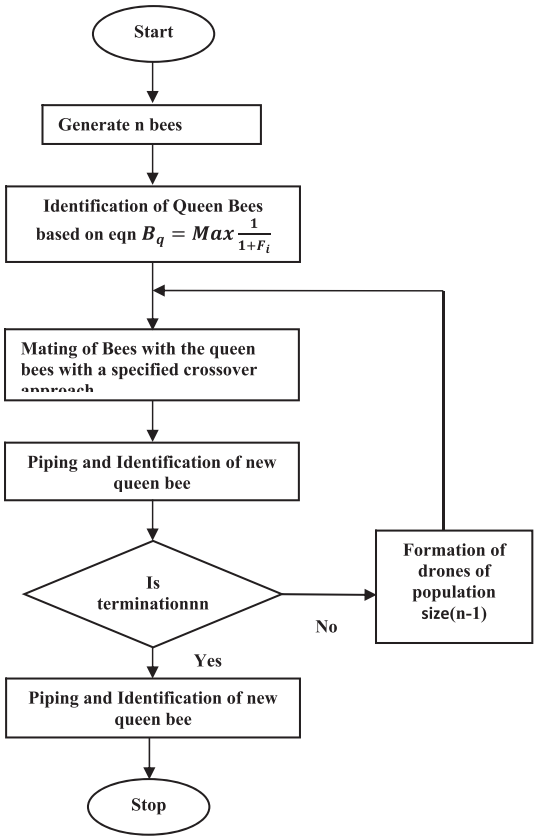


FIGURE 5 Flowchart of QBGA tuning algorithm

TABLE 2 Hardware specification

Rating	2 kVA, 3-Phase, 140 V(p-p), 50 Hz system
IGBT	CT60AM-Semikron, 600 V, 100A-Semikron
Firing pulse generation	Xilinx XC3SD1800A – FG676-4 Spartan 3A DSP FPGA
CT / PT	LTS 25 NP - 25 Amps / LV 25 - NP (0-500 V)
Capacitor	3300 μF, 900 V
Driver circuit	TLP 250 IC

voltages. The signals received from the transducers are converted to -10 V to +10 V range that is suitable for analogue channels of the FPGA through the signal conditioning circuit. The outputs of these circuits are given to 12-bit bipolar analogue-to-digital converters (AD7366IC), and these digital data are given to the FPGA processor through IO lines. It has dual 12 bit/14-bit, high speed, low power successive approximation analog-to-digital converters (ADC) and throughput rate at 1 MSPS. QBGA is used to derivethe switching signals for Insulated-Gate Bipolar Transistors (IGBTs), and it is implemented using the program. For maintain the minimum current in the drive for the operation, the driver circuit (TLP 250IC) is used. It also serves to isolate the control circuit from the power circuit. To generate switching pulses for the IGBT modules of three-level diode clamped inverter, four-driver circuits are used, whichis shown in Figure 7. The range of IGBT device (CT60AM-Semikron) is based on the supply voltage and the maximum dc-link capacitor voltage and peak value of rated current during the ON state. The rating of the device is 900 V / 60 Amps, integrated fast recovery diode and the switching frequency is 20 kHz. The device is correctly mounted on the heat sink, which provides thermal conduction between devices and heat sink. The photography of the power circuit is shown in Figure 8.

5.2 | Spartan-3A DSP 1800A controller

The gains of the PI controller were initially synthesized using GA and QBGA algorithm. Then the controller was embedded digitally on an FPGA platform and implemented on a real-time SAPF system rated for 140 V, 50 Hz. The PI

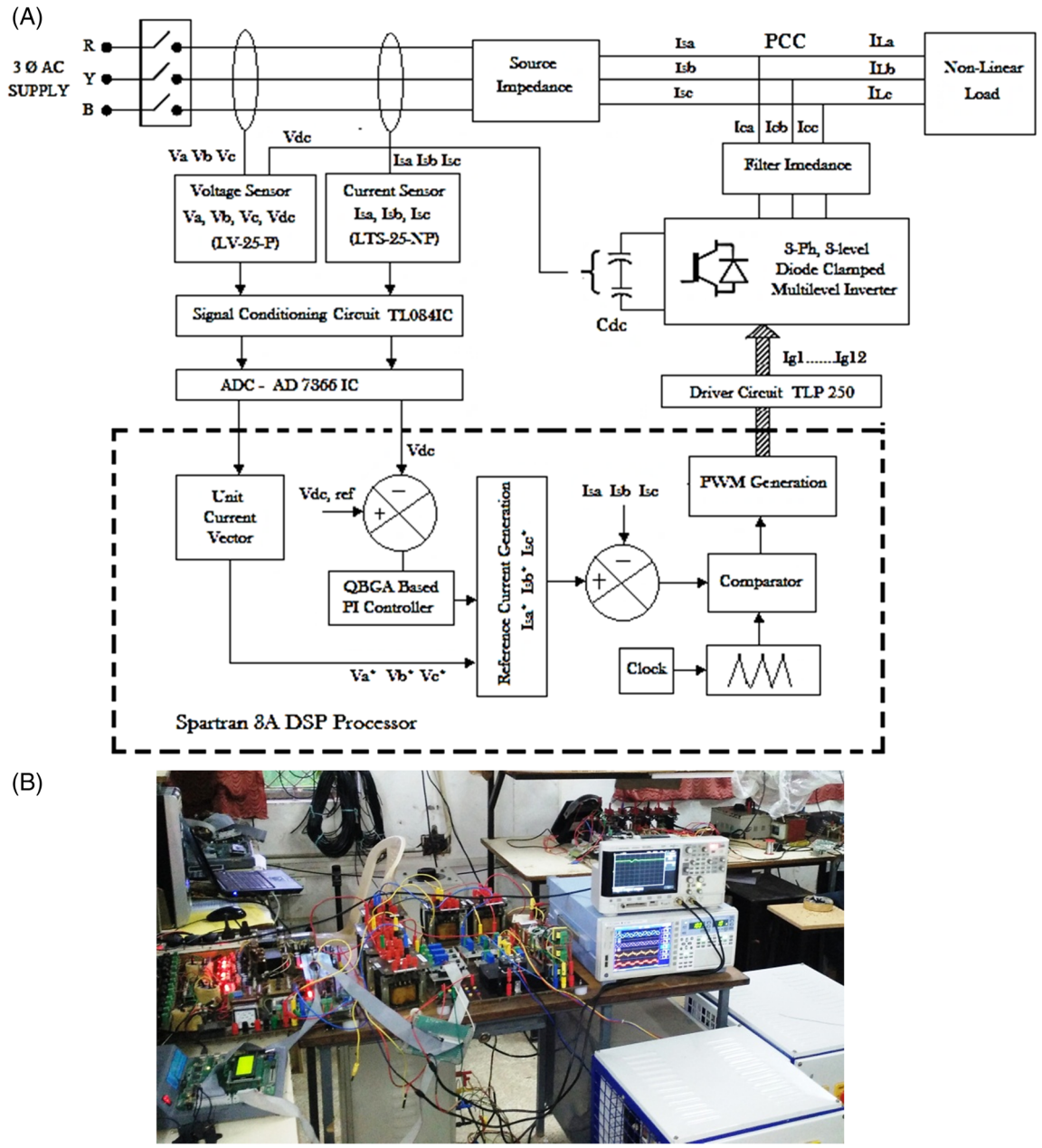


FIGURE 6 A, Hardware block diagram of SAPF. B, Photography of hardware setup

controller based on QBGA algorithm is incorporated in real-time using Xilinx XC3SD1800A - FG676-4 Spartan 3A DSP FPGA platform. The choice of processor (FPGA), feedback sensors, interfacing circuits for bringing thefeedback signals to the compatible values for the FPGA decided the speed of operation of the SAPF system. Further,

- FPGA was chosen to implement the PI controller since it provides high-speed parallel processing.
- The feedback transducers are of Hall Effect type, thereby paving the way for accurate as well as the fast measurement of system variables.
- The analogue to digital converter (12 bit) ADC7366 was chosen since it provides better resolution with fast conversion time.
- The IGBT gate drives circuit TLP250 maintains minimum current for switching operation.
- The signal conditioning unit converts the output of the transducers to +10 V to -10 V in less time, thereby supplementing the swift operation of the closed SAPF system.

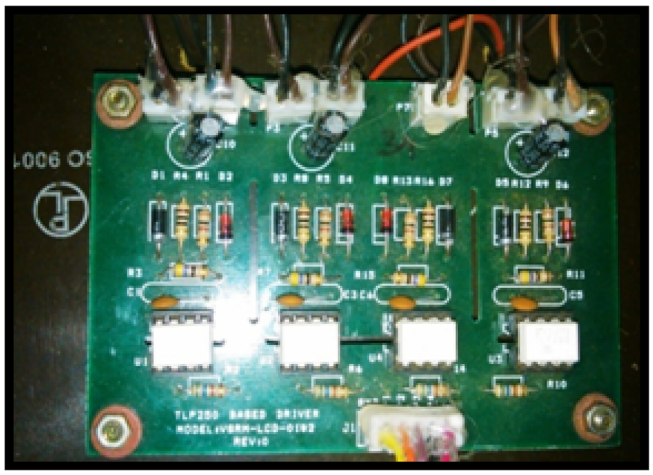


FIGURE 7 Photography of TLP 250 driver circuit

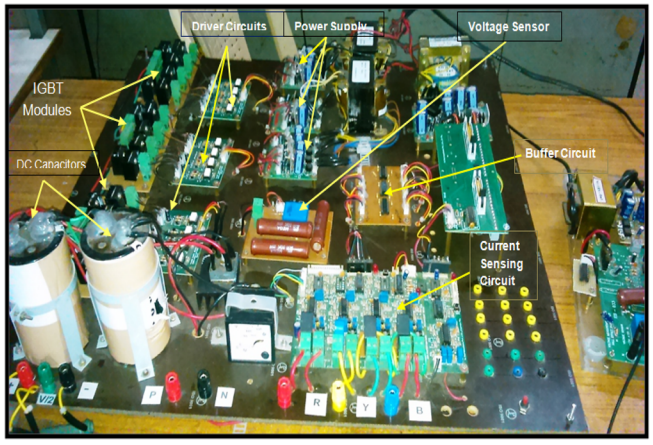


FIGURE 8 Photography of power circuit

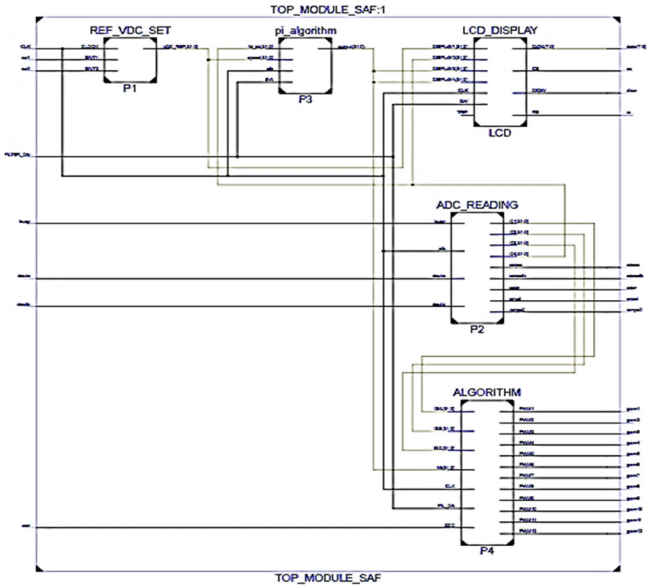
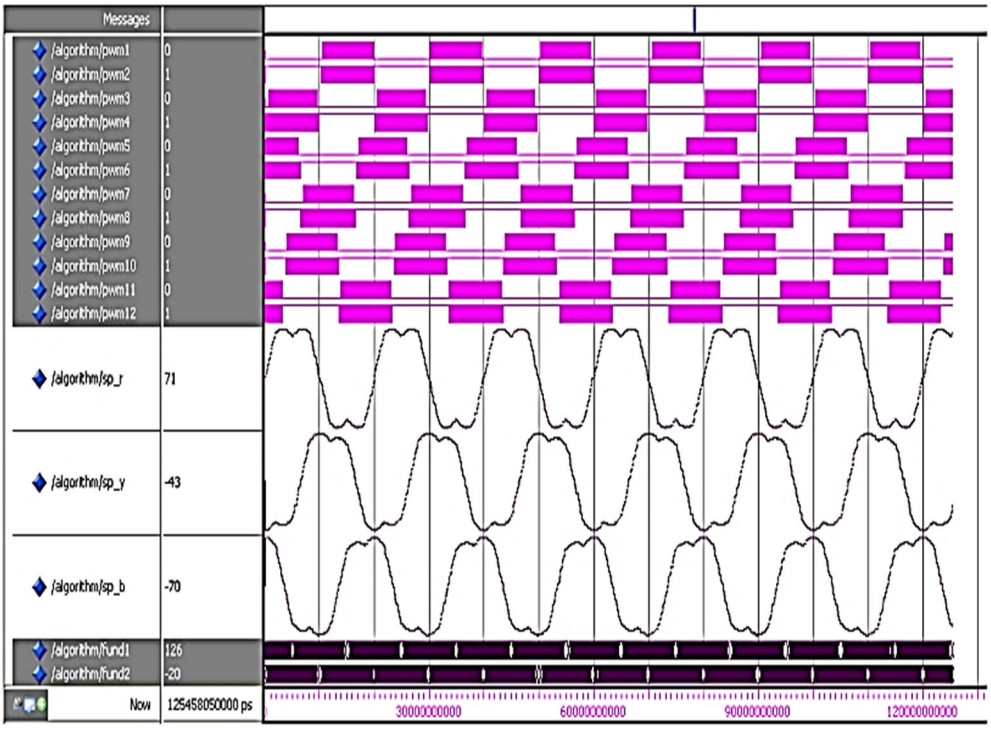


FIGURE 9 RTL view simulation of SAPF

Also, it provides four input–output banks in which two are fixed voltages and other two selectable. To support various types of applications, this processor hasnon-volatile ROM (16Mbytes parallel, and 64Mbit serial) and high-speed RAM (128Mbytes DDR2). It has Ethernet and RS232 physical layer transceivers for communication purposes. The system generator generates the VHDL program code after the verification and simulation of the controller design. The design flow in FPGA consists of the following steps.



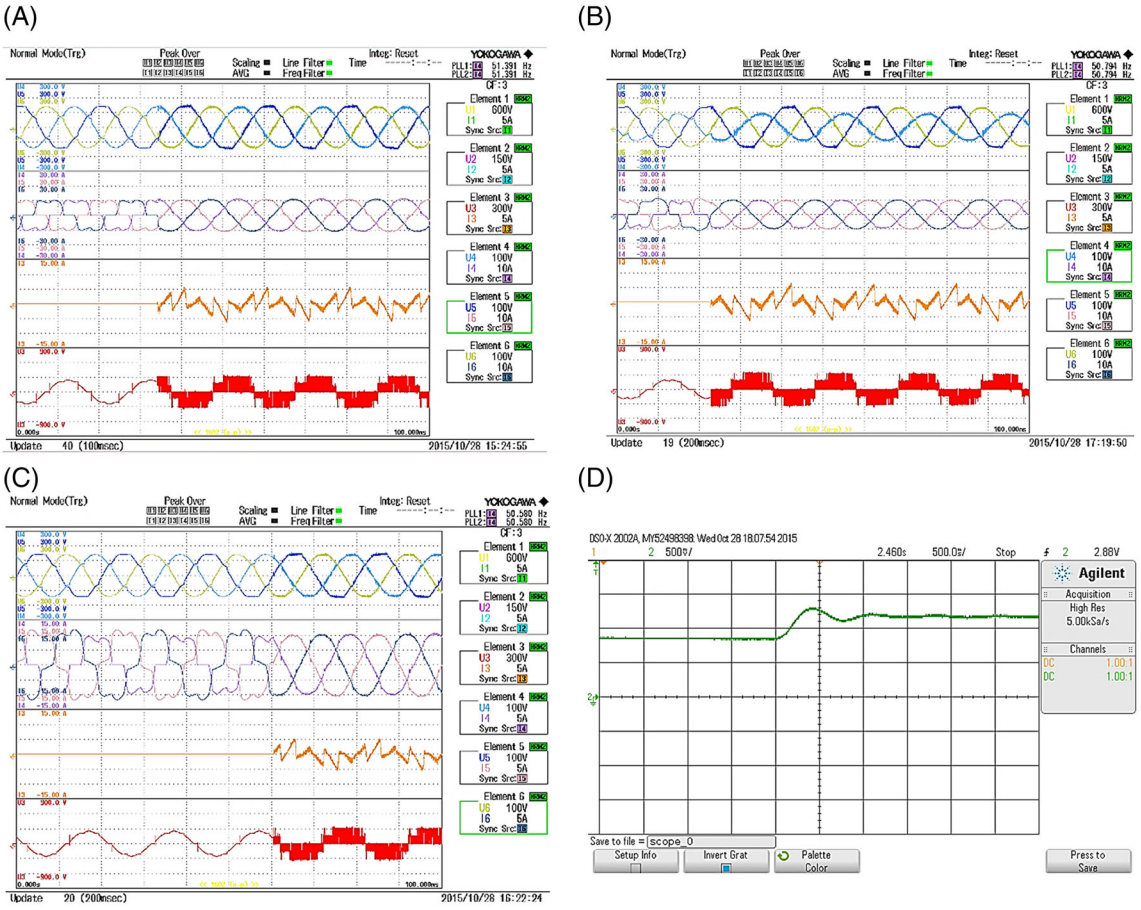


FIGURE 10 VHDL simulation results

FIGURE 11 A, Hardware outputs - steady-state conditions. B, Hardware outputs - unbalanced supply. C, Hardware outputs - unbalanced load. D, Capacitor voltage

TABLE 3 Hardware results – GA based SAPF

				Voltage at pcc, V_{pp}	Supply current (A), I_{rms}	Real power, W	Reactive power, var	Apparent power, VA	Power factor	Supply current THD %
GA Based SAPF	Without SAPF	Steady State	R-Ph	98.76	7.63	716	233	753	0.950	24.98
			Y-Ph	106.2	7.88	802	238	837	0.958	23.20
			B-Ph	100.8	7.66	733	243	772	0.949	24.39
		Unbalanced load	R-Ph	101.1	6.80	675	215	708	0.952	25.3
			Y-Ph	106.5	8.59	887	194	908	0.976	19.56
			B-Ph	101.6	8.39	809	269	852	0.948	20.63
		Unbalanced supply	R-Ph	65.88	7.09	452	-118	467	0.967	28.50
			Y-Ph	102.4	7.50	757	-132	769	0.986	22.19
			B-Ph	96.64	7.53	720	-109	728	0.988	19.81
	With SAPF	Steady State	R-Ph	98.81	8.04	787	-104	794	0.991	4.21
			Y-Ph	106.6	8.05	852	-111	859	0.991	3.79
			B-Ph	101.3	8.02	807	-99	813	0.992	3.51
		Unbalanced load	R-Ph	100.4	8.23	819	-106	826	0.991	3.71
			Y-Ph	107.3	8.34	887	-124	895	0.990	3.94
			B-Ph	102.2	8.31	844	-100	850	0.993	3.18
		Unbalanced supply	R-Ph	63.29	7.86	483	-118	498	0.987	4.43
			Y-Ph	102.3	8.16	823	-138	835	0.989	3.91
			B-Ph	97.09	8.15	786	-93	791	0.993	3.17

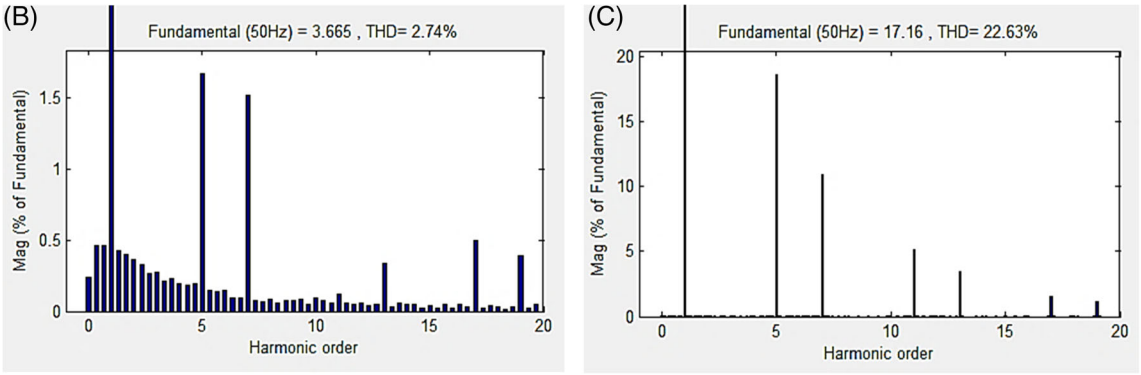


FIGURE 12 A, Evaluation of ISE, K_P and K_i values. B, THD of supply current with SAPF. C, THD of supply current without SAPF

TABLE 4 Simulation parameters

Iterations	**50**
Population size	10
Crossover probability	0.8
Mutation probability	0.2
Fitness Scaling	Rank
Selection	Roulette wheel
Time limit	Infinite
Search space	[0 0] to [5 150]
Dimension	2

- Design entry and synthesis
- Design implementation
- Design verification

The FPGA controller generates the switching pulses for the three-level multilevel inverter by sensing the input source current and voltages. These pulses are connected to the switching devices through the driver circuit and the optoisolator circuit. The input signals (i_{sa}, i_{sb}, i_{sc}, V_{dc}, V_{sa}, V_{sb},V_{sc})wereconverted to fixed-point for digital-design. The switching pulses are generated by comparing the reference signal and triangular signal using min-max control techniques. Xilinx-block set is used to design the entire control algorithm, and it provides the VHDL code. The VHDL code is tested and complied in the Xilinx-ISE 10.1 project navigator. The analysis, synthesis and RTL schematic view of the HDL is executed, as shown in Figure 9. The current reference generation, along with switching pulses through the usage of VHDL simulation and shown in Figure 10.The maximum duration of the ON period of individual switches and delay in switching on the anti-parallel switches are considered in the implementation phase. Those values are depending on the type of switching elements used in the hardware.

(Switching pulses and reference current)

5.3 | Hardware and simulation results

5.3.1 | Hardware results - genetic algorithm based SAPF

This section proceeds the implementation of the SAPF for compensating harmonics and reactive power at PCC. The gain values of the PI controller areestimated using GA, and it is validated through the experimental setup. Indirect current control approach for generating the PWMswitching pulses for the three-level multilevel inverter is made by using the space vector modulation technique and GA.The non-linear load distorts the currents at PCC. Figure 11A shows that the three-phase voltages, supply current, filter current and inverter output voltage waveforms under steady-state

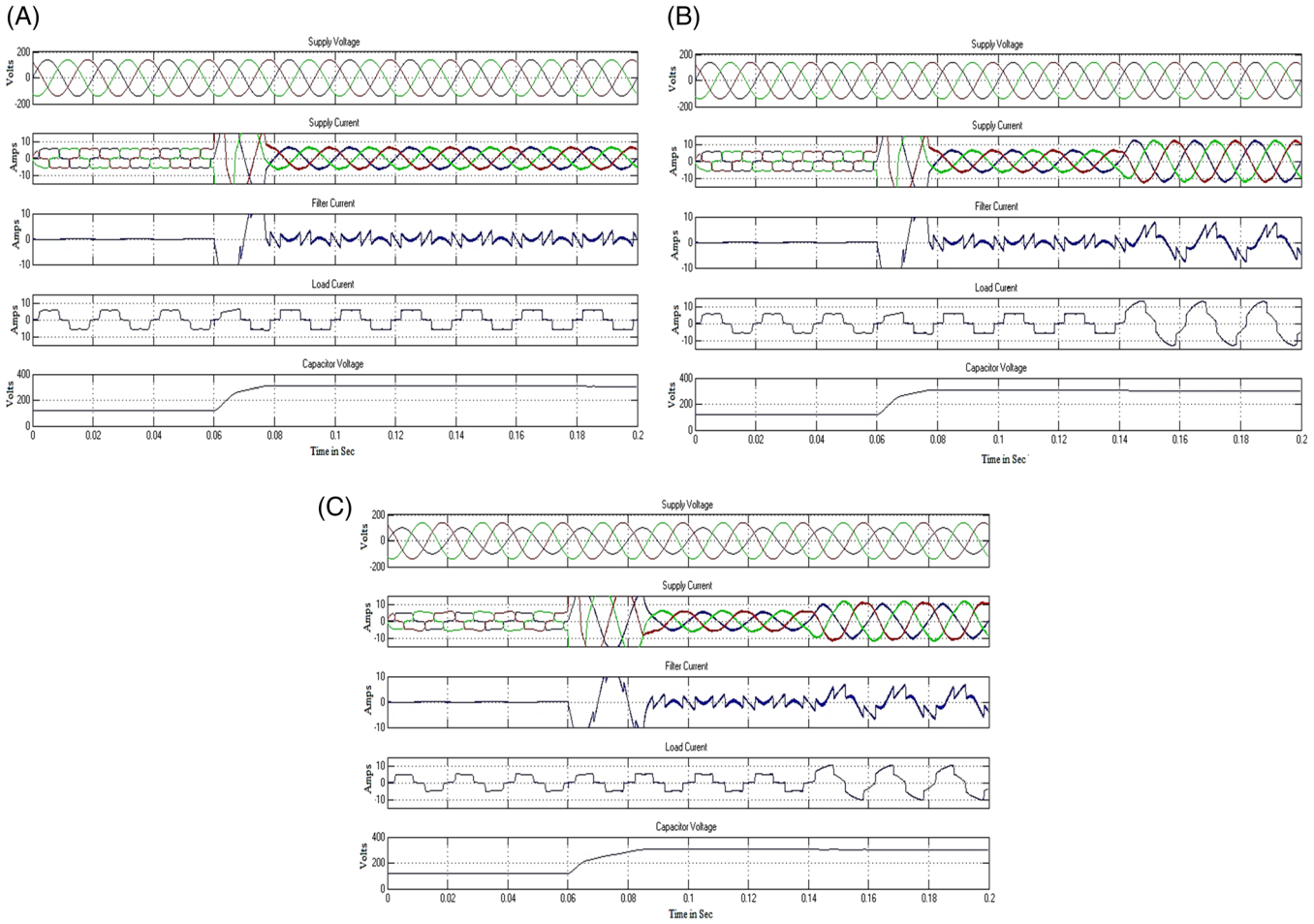


FIGURE 13 A, Steady state condition. B, Dynamic condition - increasing load. C, Dynamic condition - unbalanced supply

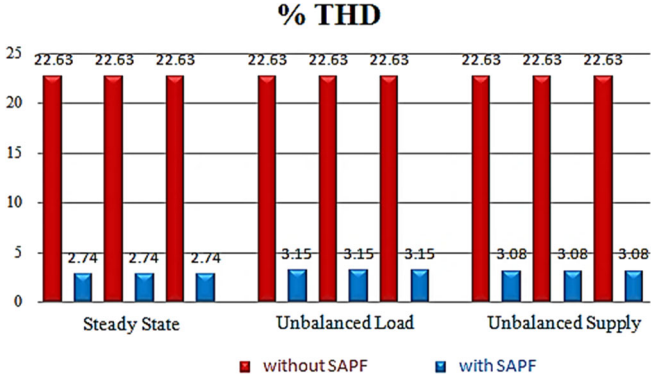


FIGURE 14 Simulation results (% THD with and without SAPF)

conditions before and after the SAPF are presented. In this hardware output, it is clearly showing that when the SAPF is connected after 1.5 cycles, the supply current is transformed into sinusoidal and balanced.

To test the performance of the SAPF system under unbalanced supply situation, the source peak voltages of R-ph, Y-ph and B-Ph are 140 V, 140 V and 100 V selected. It is clearly observed that the SAPF system maintains the source current be sinusoidal and balanced after turn on the filter after one cycle is shown in Figure 11B. The supply currents are balanced and sinusoidal even after the load gets unbalanced currents such as 6.80A, 8.59A and 8.39A are illustrated in Figure 11C. The voltage across the capacitor is presented in Figure 11D. The THD of the supply currents of ph-a, ph-b, ph-c are found to be 4.21%, 3.79%, 3.51% under steady-state after connecting the SAPF at PCC and power factor of the system is also improved close to unity. The numerical values of the line voltages at PCC, supply current, real power,

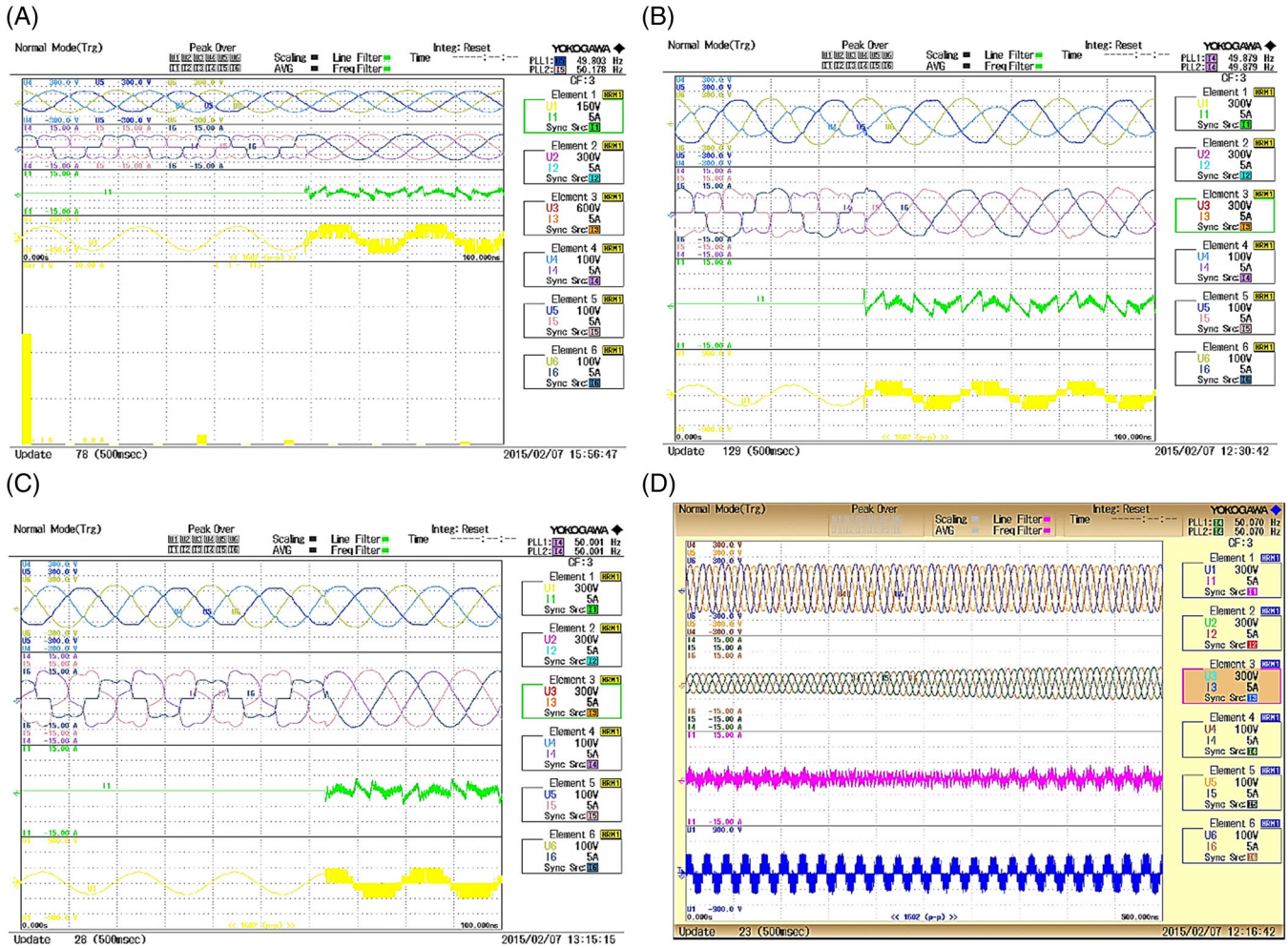


FIGURE 15 A, Hardware output - steady-state. B, Hardware output - unbalanced supply. C, Hardware output - unbalanced load. D, Hardware output - increasing load

reactive power, apparent power, power factor and % THD obtained from the hardware modules are tabulated in Table 3.

5.3.2 | Simulation results -genetic algorithm based SAPF

The performance of the SAPF is simulated through MATLAB/SIMULINK software.[22-25] The overall system consists of a three-phase three-level diode clamped inverter, source impedance, filter impedance and a nonlinear load. The synthesis of PI controller gains is based on an optimization algorithm which, given the system complexity, is non-convex in nature. Hence, by employing meta-heuristic techniques like Genetic Algorithm, the solution for the global minimum is deduced. The Figure 12A shows how the objective function gets minimized with the evolution of each generation of chromosomes in GA, and it is observed from the graph that the solution converges to global optimum within 10 generations. The simulation parameters are given in Table 4. The supply current THD with and without SAPF is shown in Figure 12B,C, respectively. The SAPF is enabled at $t = 0.6$ *seconds*; it is studied that the supply current is sinusoidal and balanced even the load becomes steady-state and increasing load is shown in Figure 13A,B, respectively. It is observed that even when the supply gets unbalanced situation, the supply current is balanced and sinusoidal, which shows that the reliability of SAPF is given in Figure 13C. The supply current THD observed from simulations with and without SAPF is presented in Figure 14.

TABLE 5 Hardware results – QBGA based SAPF

				Voltage at pcc, V_{pp}	Supply current (A), I_{rms}	Real power, W	Reactive power, var	Apparent power, VA	Power factor	Supply current THD %
QB assisted GA Based SAPF	Without SAPF	Steady State	R-Ph	103.8	5.89	580.66	180.14	607.96	0.955	25.27
			Y-Ph	102.1	5.90	578.59	169.39	602.88	0.957	26.88
			B-Ph	106.7	6.06	642.21	180.76	667.15	0.962	25.01
		Unbalanced load	R-Ph	98.5	6.49	605.57	-137.54	620.99	0.975	16.26
			Y-Ph	97.8	6.41	545.70	174.65	572.96	0.952	18.16
			B-Ph	98.7	4.62	440.15	119.40	456.06	0.965	23.93
		Unbalanced supply	R-Ph	70.64	4.67	303.73	129.02	329.99	0.920	31.59
			Y-Ph	104.40	5.57	560.94	155.97	582.22	0.963	25.08
			B-Ph	109.68	5.85	617.70	177.40	642.67	0.961	19.47
	With SAPF	Steady State	R-Ph	102.95	5.92	608.64	42.18	610.10	0.997	2.97
			Y-Ph	100.07	6.22	621.16	49.41	623.12	0.996	2.61
			B-Ph	106.10	6.18	655.10	30.84	655.82	0.998	2.56
		Unbalanced load	R-Ph	99.59	5.88	561.25	-37.44	562.50	0.997	2.49
			Y-Ph	97.45	6.10	557.32	-49.45	559.51	0.996	2.62
			B-Ph	98.77	5.93	584.67	45.57	586.45	0.997	2.05
		Unbalanced supply	R-Ph	69.25	5.15	354.58	-43.91	357.28	0.992	3.88
			Y-Ph	104.24	5.75	596.25	-64.65	599.74	0.994	3.16
			B-Ph	109.10	5.76	633.96	29.61	634.65	0.998	2.70

TABLE 6 Simulation parameters using QBGA

Iterations	50
Population size	10
Crossover probability	0.6
Mutation probability	0.1
Recombination probability	0.8
Search space	[0 0] to [5 150]
Dimension	2

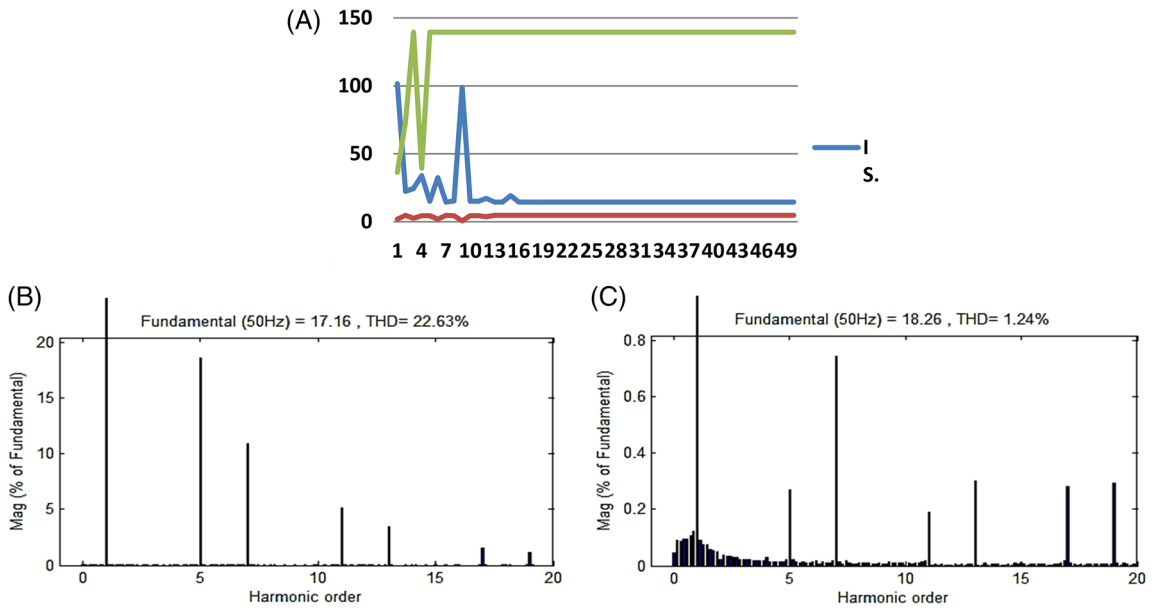


FIGURE 16 A, Evaluation of ISE, K_P and K_i values. B, THD of supply current without SAPF. C, THD of supply current with SAPF

5.3.3 | Hardware results - QBGA based SAPF

The three-phase diode bridge connected to R-L load is chosen as a representative nonlinear load for the study of SAPF. The experimental set up was started without SAPF, and after all the initial transients died down (roughly it takes about three cycles), SAPF was connected to infer its influence on the quality of the current waveform (which was non-sinusoidal before plugging in the SAPF). The current waveform becomes sinusoidal and balanced after the SAPF was connected. The line to line voltages, supply current, filter current and inverter output voltage waveforms under static load conditions with balanced supply are presented in Figure 15A. In this hardware output, it is clearly showing that when the SAPF is connected after 3 cycles, the supply current is transformed into sinusoidal and balanced. To test the performance of the SAPF system under unbalanced supply situation, the source peak voltages of R-ph, Y-ph and B-Ph are 140 V, 140 V and 100 V selected. It is observed that the SAPF system maintains the source current be sinusoidal and balanced after turn on the filter is shown in Figure 15B. The supply currents are balanced and sinusoidal even after the load gets unbalanced currents such as 6.4A, 6.4A and 4.6A are illustrated in Figure 15C.

The THD of the supply current is reduced to below 5%. In addition, the power factor of the system is improved close to unity after connecting the SAPF at PCC. The balanced load is increased gradually, as shown in Figure 15D. The numerical values of the line voltages at PCC, supply current, real power, reactive power, apparent power, power factor and % THD obtained from the hardware modules are tabulated in Table 5.

5.3.4 | Simulation results – QBGA based SAPF

The performance of the SAPF is simulated through MATLAB/SIMULINK software. The overall system consists of a three-phase three-level diode clamped inverter, source impedance, filter impedance and a nonlinear load. The reference

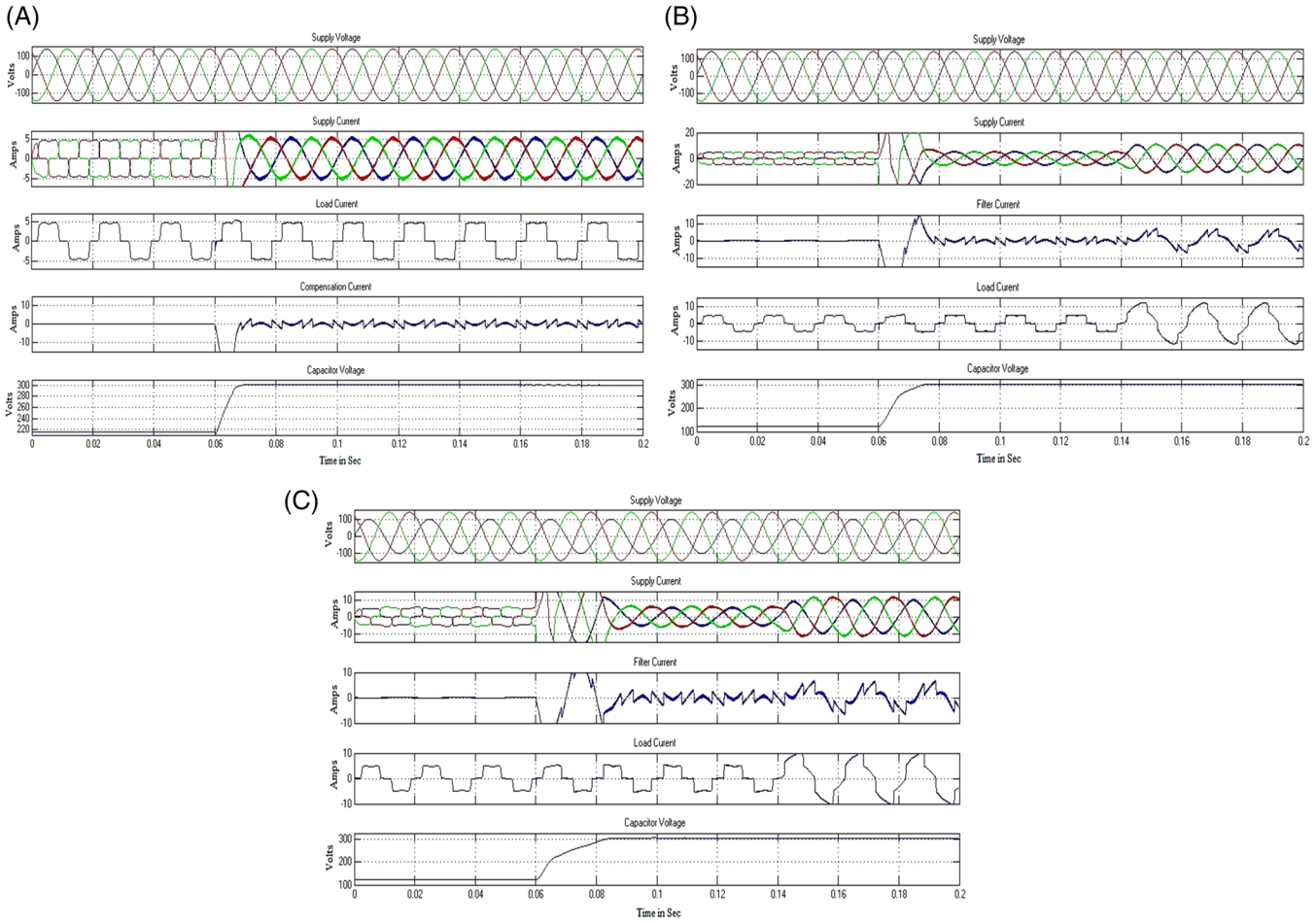


FIGURE 17 A, Simulation output - steady-state. B, Dynamic performance - increasing load. C, Dynamic performance -unbalanced supply

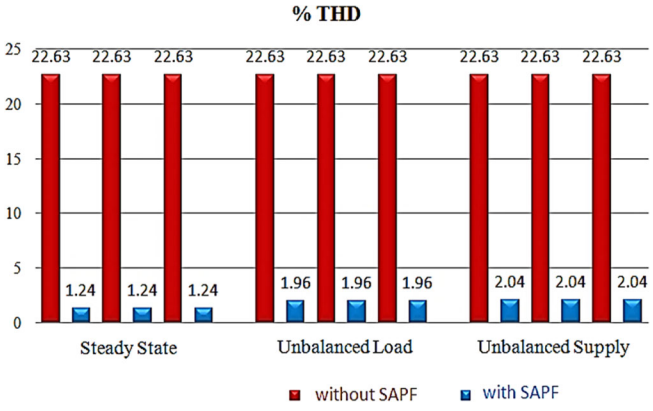


FIGURE 18 QBGA Simulation results - % THD with and without SAPF

current is generated through the QBGA optimized PI controller, and PWM pulses are generated through the Min-Max modulation technique. The parameters used in the simulation for the proposed system are given as follows: Input supply voltage is 140 V_{pp}, 50 Hz and source impedances are Rs = 0.1 Ω and Ls = 0.002H. The resistance of 0.1 Ω and inductance of 0.66 mH are connected at PCC as filter impedances. The three-phase diode bridge along with the resistance of 50 Ω and inductance of 40 mH act as nonlinear loads. The value of the DC capacitor is 3300 μF, and the reference voltage is fixed as 300 V. QB assisted GA is applied for controlling a SAPF for mitigating the harmonic and reactive power drawn from the load. The parameters considered for the simulation using QBGA is tabulated in Table 6.

The control of the SAPF system is achieved through the QBGA based PI controller to study the performance of the system with static and dynamic conditions. The optimum value of ISE, K_p and K_i tuning parameters obtained after

TABLE 7 Comparisons of results

Control scheme			Supply current THD in % with SAPF								
			Steady state			Transient state					
			Balanced supply			Unbalanced supply			Unbalanced load		
			Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Genetic Algorithm		Simulation	2.74	2.74	2.74	3.08	3.08	3.08	3.15	3.15	3.15
		Hardware	4.21	3.79	3.51	4.43	3.91	3.17	3.71	3.94	3.18
		Settling Time	0.17 s			0.25 s			0.23 s		
Queen Bee GA		Simulation	**1.24**	**1.24**	**1.24**	**2.04**	**2.04**	**2.04**	**1.96**	**1.96**	**1.96**
		Hardware	**2.97**	**2.61**	**2.56**	**3.88**	**3.16**	**2.70**	**3.5**	**3.12**	**3.01**
		Settling Time	**0.008 s**			**0.23 s**			**0.23 s**		
The work of[26] (PSO)		Simulation	**2.04**	**2.04**	**2.04**	Not Considered					
		Hardware	**3.51**	**3.13**	**3.01**	Not Considered					
The work of[9] (Fuzzy-GA)		Simulation	2.41	2.41	2.41	Not Considered					
		Settling Time	0.08 s			Not Considered					
The work of[10] (Adaptive-Fuzzy Sliding Control)		Simulation	1.59	1.59	1.59	Not Considered					
		Settling Time	0.01 s			Not Considered					
The work of[12]	PI-MPC control	Simulation	4.65%			5.32%					
	RECKF-MPC	Simulation	4.46%			4.67%					
		Settling Time	0.02 s (approx.)			0.05 s (approx.)					

Significance for bold values are result of our work.

50 iterations are 14 539, 4.72394, and 139.408, respectively. The evaluation of tuning parameters is mentioned in Figure 16A. The value of the THD of supply current is raised to 22.63%, as shown in Fig. The load draws 16B and the reactive power, thereby the power factor of the system is low. At time $t = 0.06$seconds, the filter circuit is enabled, and the supply current THD is reduced to 1.24% as displayed in Figure 16C and the corresponding power factor is improved to 0.989 lag from 0.9512 lag. Owing to the occurrence of the nonlinear load of 0.6 kW connected at PCC, the source current waveform contains harmonics and non-sinusoidal. Figure 17A represents the supply voltage (v_{sa}), supply current (i_{sa}), compensation current (i_{ca}), load current (i_{La}), and the voltage across the capacitor (V_{dc}) with and without SAPF under static condition.

To verify the SAPF during dynamic behaviours, the load current is changed perturbed from 4.5A to 7A at $t = 0.14$ *ms*. When the load current changes, the voltage between the capacitor changes can be estimated by QBGA algorithm and adjusts the peak value of the reference currents. Figure 17B shows the supply voltage (v_{sa}), supply current (i_{sa}), compensation current (i_{ca}), load current (i_{La}) and voltage across the capacitor (V_{dc}) with and without SAPF under dynamic conditions. Figure 17C represents the performance of the SAPF under unbalanced supply condition. It is concluded that the SAPF performs satisfactorily under balanced and unbalanced conditions. The supply current THD with and without SAPF is illustrated in Figure 18.

Table 7 shows a comparison of supply current THDs and settling time of DC capacitor under balanced supply, unbalanced supply and unbalanced load after SAPF is switched ON. Hardware results for the above conditions are also presented. By comparing the simulation results, it is observed that QBGA is a better algorithm since it provides more effective compensation than reflects in lower THD values than the GA algorithm. The hardware implementation is to verify the QBGA algorithm. Furthermore, similar results available in the literature are also shown in Table 7 to underline the efficacy of QBGA technique.

Queen Bee GA based tuning method is superior in ideal case/simulation as compared to GA, Fuzzy based GA,[9] PSO[26] and Adaptive-fuzzy sliding control.[10] The percentage of error in the hardware result concerning simulation is computed as $\frac{\%THD_{hw}-\%THD_{sim}}{\%THD_{sim}} \times 100$. There exists a maximum error of 1.4%, that is, the percentage of THD in supply current present in the hardware is 1.4% more than the simulation result. This error could be further reduced if an appropriate switching characteristic and switching circuit impedance are used during the tuning face whereas the works of[9,10,12] are presented only the simulation results.

6 | CONCLUSION

To achieve better control and utilization of SAPF, a novel Queen Bee assisted GA is proposed in this work. This scheme utilizes the estimation of the fundamental phase component along with the estimation of load current using QBGA algorithm. The performance of the SAPF using Queen Bee assisted GA algorithm was implemented to find the optimum value of proportion and integral gains of the PI controller. A parallel simulation using GA based SAPF is carried out on the same data, and the results were compared with those of the proposed QBGA technique. It is shown that the proposed QBGA fares better as a tuning method. An experimental model has been developed and implemented in QBGA, and their results are also presented. The possibility of extending the proposed control technique to SAPF system with time-varying parametric uncertainties will be explored in future.

PEER REVIEW

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